## 2019 IEEE Asian Solid-State Circuits Conference
### Technical Program

### Day One (Nov. 4, 2019)

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Kenneth K. O, University of Texas at Dallas  
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| 10:50-12:20 (90) | **Tutorial 2**  
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Masato Motomura, Tokyo Institute of Tech.  
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Dr. Yasunori Mochizuki, NEC Fellow
NEC Corporation
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Day 1, November 4, 2019 (Monday)

[Tutorial 1]
TITLE: On-Chip Millimeter Wave Voltage Measurements for Debugging, Built-in Self-Test and Self-Healing
DATE/TIME: November 4, 2019 (Monday) / 9:00 AM – 10:30 AM
ROOM: 7404 & 7504
SPEAKER: Prof. Kenneth O, University of Texas at Dallas, USA

Abstract:
Traditional high frequency testing using probes and external instruments in conjunction with de-embedding is unacceptable in high volume testing of millimeter wave (mm-wave) CMOS integrated circuits for the emerging consumer applications. The cost, test time, and the level of required sophistication for the traditional techniques are too high. In addition, debugging circuit behaviors by measuring internal node voltages using the traditional techniques is impractical because of the parasitics of probe pads and impact of probe landing. Lastly, due to use of components with smaller physical dimensions, mm-wave circuits are more sensitive to process variations. The first two challenges can be circumvented by utilizing high impedance broadband root mean square detectors that has negligible impact to operation as part of the circuit to enable measurements of millimeter wave voltages using low frequency measurements. The third can be mitigated by using the detectors along with on-chip tuning elements. In fact, this can allow use of higher Q circuits with improved power efficiency. This tutorial discusses devices in CMOS for implementing the detectors, design considerations and examples of how these detectors can be used in circuits operating at 30 to 300 GHz.

Biography:
Kenneth O received his Ph.D. degree in Electrical Engineering and Computer Science from MIT in 1989. From 1989 to 1994, He worked at Analog Devices Inc. developing sub-micron CMOS processes and high speed bipolar and BiCMOS processes. He was a professor at the U. of Florida, Gainesville from 1994 to 2009. He is currently the Director of Texas Analog Center of Excellence and TI Distinguished University Chair Professor at the U. of Texas at Dallas. His research group is developing circuits, components and systems operating at frequencies up to 40THz using silicon IC technologies. Dr. O is the Vice President and President Elect of the IEEE Solid-State Circuits Society. Dr. O has received the 2014 Semiconductor Research Association University Researcher Award. Prof. O is an IEEE Fellow.
Abstract:
Thanks to the enormous progress and success of deep neural networks (DNNs), computer architecture research has been regaining its past "excitement" again recently: a lot of architectural proposals have been proposed for the accelerated execution of the inference or training of DNNs, especially at the edge. Most of them have common architectural features: i.e., hardware-oriented, reconfigurable, domain-specific, and in/near-memory. This tutorial will try to supply 1) background knowledge to understand such DNN architectures, 2) insights on why they are happening, 3) what are the recent findings, and 4) where this architectural innovation will be heading. This tutorial will also cover four such research examples that the presenter’s teams have developed in the past few years: a) binary reconfigurable in-memory DNN accelerator (VLSI 2017), b) log-quantized and 3D-memory stacked DNN accelerator (ISSCC 2018), c) dynamically reconfigurable AI engine (VLSI 2018) (DRP), and d) an error-amortizing binary DNN architecture (FPT 2018).

Biography:
Masato Motomura received B.S. and M.S. in 1985 and 1987, respectively, and Ph.D. of Electrical Engineering in 1996, all from Kyoto University. He joined NEC research laboratories in 1987, where he worked on various hardware architectures including multi-thread parallel processors, memory-based processors, and reconfigurable systems. From 2001 to 2008 he led research and productization of DRP (dynamically reconfigurable processor) that he invented. He was also a visiting researcher at MIT Laboratory for Computer Science from 1991 to 1992. He became a professor at Hokkaido University in 2011, and then a professor at Tokyo Institute of Technology from 2019 where he is currently leading AI Computing Research Unit. He won the IEEE JSSC Annual Best Paper Award in 1992, IPSJ Annual Best Paper Award in 1999, and IEICE Achievement Award in 2011, ISSCC Silkroad Award as the last author in 2018, respectively. He is a member of IEEE, IEICE, IPSJ, and EAJ.
TITLE: Bringing back Pipelined ADCs in the Era of SAR ADCs
DATE/TIME: November 4, 2019 (Monday) / 1:40 PM – 3:10 PM
ROOM: 7404 & 7504
SPEAKER: Prof. Seung-Tak Ryu, KAIST, South Korea

Abstract:
While SAR ADCs have become one of the most popular ADC architectures during the past decade owing to its compactness and power-efficiency in advanced CMOS processes, their limited conversion rate still remains as a major design bottleneck even with time interleaving (TI), especially in implementing high-resolution. Meanwhile, pipelined ADCs have been evolved to circumvent the opamp-based power-hungry residue generation. Often with SAR ADCs as sub-stages, recently, pipelined ADCs could achieve both high conversion rate and power efficiency. As pipelining also alleviates the calibration burden of channel-mismatch in TI ADCs owing to the reduced number of high-speed channels, this architecture needs to be improved continuously. Based on this perspective, this tutorial aims to provide knowledge on pipelined ADCs including the operational principle, the importance of residue accuracy and major error sources, history of design innovations focusing on key circuit blocks and architectural modification, and recent remarkable design examples.

Biography:
Seung-Tak Ryu (M'06–SM'13) received the M.S. and Ph.D. degrees from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1999 and 2004, respectively. He was with Samsung Electronics in Kiheung, Korea from 2004 to 2007. From 2007 to 2009, he was with the Information and Communications University, Daejeon, Korea, as an Assistant Professor. He has been with the Department of Electrical Engineering, KAIST, Daejeon, Korea, since 2009, where he is currently an Associate Professor. His research interests include analog and mixed-signal IC design with an emphasis on data converters.

Prof. Ryu served as a Technical Program Committee (TPC) member of the ISSCC, and he is now serving as has been serving on the A-SSCC. He is now serving as an Associate Editor of the IEEE Solid-State Circuits Letters.
Abstract:
Memory has proven a major bottleneck in the development of energy-efficient chips for IoT applications and artificial intelligence (AI). Recent emerging memory devices not only serve as memory macros, but also enable the development of computing-in-memory (CIM) for IoT and AI chips. In this tutorial, we will review recent trend of memory and AI+IoT chips. Then, we will examine some of the challenges, circuits-devices-interaction, and recent progress of silicon-proven SRAM and emerging-memory based CIMs for IoT and AI chips.

Biography:
A Distinguished Professor at National Tsing Hua University, Taiwan. Since 2010, Dr. Chang has authored or co-author more than 50+ top conference papers (including 18 ISSCC, 21 VLSI Symposia, 9 IEDM, and 5 DAC). He has been serving as an associate editor for IEEE TVLSI, IEEE TCAD, and a guest editor of IEEE JSSC. He has been serving on TPC for ISSCC, IEDM (Ex-com and MT chair), DAC (sub-com chair), A-SSCC, and numerous conferences. He has been a Distinguished Lecture (DL) speaker for IEEE Solid-State Circuits Society (SSCS) and Circuits and Systems Society (CASS), and the AdCom member of IEEE Nanotechnology Council. He has also been serving as the Program Director of Micro-Electronics Program of Ministry of Science and Technology (MOST) in Taiwan during 2018-2020, Associate Executive Director for Taiwan’s National Program of Intelligent Electronics (NPIE) during 2011-2018. He is the recipient of the Outstanding Research Award of MOST-Taiwan and other national awards. He is a Fellow of the IEEE.
Day 2, November 5, 2019 (Tuesday)

Opening Ceremony
DATE / TIME: November 5, 2019 (Tuesday) / 08:30 AM - 08:50 AM
ROOM:7401-7403 & 7501-7503

Session P1: Plenary
DATE / TIME: November 5, 2019 (Tuesday) / 08:50 AM – 10:20 AM
ROOM:7401-7403 & 7501-7503
CHAIR: Mototsugu HAMADA, Keio Univ.

[Plenary Talk 1]
TITLE: What are the driving forces of DRAM?
DATE/TIME: November 5, 2019 (Tuesday) / 08:50 AM – 09:35 AM
SPEAKER: Mr. Yiming Zhu, Chairman & CEO, ChangXin Memory Tech., China

Abstract:
China is rising as one of the biggest IC consumers in past several years. Due to widely well accepted mobile ecosystem, the exploding Chinese mobile payment economy is currently sized at more than 6 trillion US dollars per year, driving a massive demand for real time and secure financial transactions. To meet the exacting needs of this exploding e-commerce industry, both consumer mobiles and data centers require ever increasing amounts of advanced memory. In this session, CXMT Chairman and CEO, Yiming Zhu will share on how the China memory industry had been addressing challenges in technology, supply chain and current progresses to meet the growing needs of the new digital world.

Biography:
YiMing Zhu joined CXMT in 2018 as CEO, and then assumed Chairman in 2019. Before CXMT, Mr. Zhu was founder, Chairman and CEO of GigaDevice Semiconductor Inc. (SSH:603986). He was credited with a pioneer of China Memory Industry; He started his career in USA as a R&D engineer before he founded GigaDevice. Yiming received his Bachelor and Master Degree from Tsinghua University and Master Degree from State University of New York at Stony Brook.
Abstract:
ICT industry is taking a new turn driven by the development of artificial intelligence and network systems. Artificial intelligence has already been used directly and indirectly in everyday life, and the world we live in is becoming more and more smart. However, there are still many tasks to solve. In the future, the artificial intelligence computing system will play a pivotal role in realizing Next Smart Society, so a lot of research is underway in the related industries to improve the performance dramatically.
While various approaches are being developed to utilize artificial intelligence systems, data bottlenecks between artificial intelligence processors and memory are still bottlenecks to improve system performance. In addition, increase in power consumption due to increased bandwidth remains a problem to be solved.
In this keynote speech, I would like to present the direction of memory development for Next Smart Society. Currently, the memory industry is developing a high bandwidth memory to meet the system requirements to contribute to system performance improvement, but it is time to develop more innovative memory technology to meet the requirements of the artificial intelligence system.
In order to do this, we need not only to improve the memory itself but also to combine logic processor with memory to reduce unnecessary bandwidth usage by adjoining memory near processor with diversification of System in Package assembly technology. Furthermore, it is necessary to change the architecture of computing system so that collaboration with people from adjacent fields is essential.

Biography:
KyoWon JIN became General Manager of DRAM Development & Business in SK hynix Inc. in December 2018 after his 2 years tenure as General Manager, while retaining the position of Executive Vice President of Quality & Reliability Assurance since December 2016.
Prior to his current position, he was Senior Vice President of NAND Development Division from July 2014 and Flash Product Planning from December 2013.
Mr. Jin became a Senior Vice President of Product Planning in August 2009, and he was a Vice President and took the position of DRAM Development Division in charge of DRAM product development from March 2003 to January 2008.
He has been responsible for leading initiatives in the research and development of semiconductor memory for mobile, graphics, server, and future applications. In addition, he had been working for managing quality and reliability of semiconductor memory.
He has worked for semiconductor industry since 1985, acquiring more than 35 years of experience. Mr. Jin has a bachelor's degree in Physics from Seoul National University.
A 45nm 76-81GHz CMOS Radar Receiver for Automotive Applications
Debabriya Sahu, Rittu Sachdev-Singh, Harikrishna Parthasarathy, Rohit Chatterjee, Brian Ginsburg, Daniel Breen, Karan Bhatia, Sudhir Polarouthu, Vimal Edayath, Bhupendra Sharma, Meghna Agarwal, Karthik Subburaj, Anjan Prasad, Shankar Ram, Cathy Chi, Ross Kulak, Vijay Raval, Neeraj Nayak

Abstract:
This paper describes the design and performance of a 45nm CMOS (fT=160GHz) 76-81GHz radar receiver used in Advanced Driver-Assistance Systems which utilizes Frequency-Modulated Continuous Wave (FMCW) synthesis. The receiver achieves 18dB noise figure and -7dBm 1dB compression point consuming 225mW power. The design includes programmable gain for linearity-noise trade-off, 15MHz wide bandwidth baseband filters, 1.8G samples per second 3rd order Sigma-Delta ADC with 70dB Spurious free dynamic range. In-built safety architecture enables meeting stringent automotive safety requirements.

Keywords: millimeter wave communication, receiver, automotive electronics, FMCW, system-on-chip
control, threshold regulation

2 – 3 11:40 AM – 12:05 PM

A Cost Effective Test Screening Circuit for Embedded SRAM with Resume Standby on 110-nm SoC/MCU
Yoshisato Yokoyama, Kenji Goto, Tomohiro Miura, Yukari Ouchi, Daisuke Nakamura, Jiro Ishikawa, Shunya Nagata, Yoshiki Tsujihashi, Yuichiro Ishii
Renesas Electronics Corporation, Japan

Abstract:
A cost effective test screening circuit is proposed for ultra-low standby power SRAM. A risk that the retention test time may be increased is shown. The test circuit to discharge local powerline is newly introduced. The test circuit can turn off discharging transistor by detecting the powerlines of memory cell array voltage. The test circuit can reduce the retention test time to 1/50. SRAM macro designed using 110-nm technology has extreme low standby power of 0.28 pW/cell. The test chip was fabricated. The effects of the test circuit are confirmed by the evaluated data.

Keywords: Low standby power, Retention, Testing cost, Reverse engineering

2 – 4 12:05 PM – 12:30 PM

A 2.666GT/s 128Gb/s 14nm Memory I/O with Jitter and Crosstalk Cancellation
Harry Muljono, Kathy Peng, Linda Sun, Isaac Abraham, Charlie Lin, Yanjie Zhu, Chunrong Song
Intel Corporation, United States

Abstract:
A DDR interface that serves DDR4 and Optane DC Persistent Memory DIMMs achieves 2.666GT/s transfer rate on a state of the art 14nm Server CPU with a total of 6 channels, yielding 128GB/s data bandwidth required to fulfill high bandwidth demand of server applications. To support 2 DIMM per Channel (DPC) configuration, it utilizes three novel techniques, namely Phase Based Crosstalk Cancellation (PXC), Data Dependent Jitter Cancellation (DDJC) and un-clocked DFE architecture.

Keywords: DDR4, memory, CPU
A Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices
Takuji Miki2, Makoto Nagata2, Hiroki Sonoda2, Noriyuki Miura2, Takaaki Okidono1, Yuuki Araga3, Naoya Watanabe3, Haruo Shimamoto3, Katsuya Kikuchi3
1ECSEC, Japan; 2Kobe University, Japan; 3National Institute of Advanced Industrial Science and Technology, Japan

Abstract:
Flip-chip semiconductor packaging reduces the footprint of IC chips while leads to serious vulnerabilities against emerging backside physical security attacks. The proposed backside buried metal (BBM) structure forming a meander wire pattern detects unexpected disconnection of the wire and warns malicious attempts. Besides this BBM circuit suppresses a side-channel leakage by -26.4 dB and also blocks laser fault injection. Unlike other conventional laminate-based protection, this approach does not require additional packaging layers, resulting in only 0.0025 % size-overhead. The BBM meander was formed on the backside of a 0.13 um CMOS cryptographic chip.

Keywords: Hardware security, Physical attack, Laser fault injection, Flip-chip, Backside protection circuits

A 28nm 512Kb Adjacent 2T2R RRAM PUF with Interleaved Cell Mirroring and self-Adaptive Splitting for Extremely Low Bit Error Rate of Cryptographic Key
Xiaoyong Xue2, Jianguo Yang1, Yuejun Zhang3, Mingyu Wang2, Hangbing Lv1, Xiaoyang Zeng2, Ming Liu1
1Chinese Academy of Sciences, China; 2Fudan University, China; 3Ningbo University, China

Abstract:
This paper presents a 2T2R RRAM PUF scheme for dense and reliable cryptographic key generation in 28nm logic process. The set time mismatch in two adjacent RRAM devices is exploited for PUF output with better tolerance against PVT variability. Array architecture featuring interleaved cell mirroring improves the randomness by eliminating the systematic deviation. Self-adaptive splitting with current limiter eliminates the negative effect of mismatch in the peripheral circuits and suppresses the undue duration of large operation current. Silicon data demonstrates our RRAM PUF passes NIST test with intra-chip Hamming distance (HD) of 0, inter-chip HD of 0.496 and bit error rate of <1×10^-5@0-120 C.
Keywords: PUF, RRAM, interleaved cell mirroring, self-adaptive splitting, low bit error rate, IoT

3 – 3 11:40 AM – 12:05 PM

A 0.5V Real-Time Computational CMOS Image Sensor with Programmable Kernel for Always-On Feature Extraction
Tzu-Hsiang Hsu, Yen-Kai Chen, Tai-Hsing Wen, Wei-Chen Wei, Yi-Ren Chen, Fu-Chun Chang, Ren-Shuo Liu, Chung-Chuan Lo, Kea-Tiong Tang, Meng-Fan Chang, Chih-Cheng Hsieh
National Tsing Hua University, Taiwan

Abstract:
This paper presents a 0.5V computational CMOS image sensor (C2IS) with array-parallel computing capability for always-on feature extraction. By applying the developed pulsed-width modulation (PWM) pixel and switch-current integration (SCI), the in-sensor 8-directional matrix-parallel multiply-accumulate (MAC) operation is realized. Moreover, the analog-domain convolution-on-readout (COR) operation, the programmable 3x3 kernel with ±3-bit weights, and the tunable-resolution column-parallel ADC (1b to 8b) are implemented to achieve the real-time feature extraction without use of additional memory. The C2IS prototype has been fabricated and verified to demonstrate the raw and feature images at 480fps with a power consumption of 77/91 (uW) and the resultant FoM of 9.8/11.6 (pJ/pix/frame), respectively.

Keywords: Always-on, convolution, computational CMOS image sensor, feature extraction, processing-in-sensor

3 – 4 12:05 PM – 12:30 PM

A 16K SRAM-Based Mixed-Signal In-Memory Computing Macro Featuring Voltage-Mode Accumulator and Row-by-Row ADC
Hyunjoon Kim, Qian Chen, Bongjin Kim
Nanyang Technological University, Singapore

Abstract:
This work proposes an SRAM-based mixed-signal in-memory computing macro using a pseudo-differential voltage-mode accumulator and a row-by-row ADC. The macro consists of 128 parallel mixed-signal dot-product computing units, each with 128 bitcells (64 for synapses, 32 for ADC reference, and 32 for offset calibration). A bitcell comprises of a 6T SRAM cell, an XNOR-based binary multiplier, and a pseudo-differential voltage-mode driver. A 65nm test-chip is fabricated, and the measured energy efficiency is 87TOPS/W with 5bit ADC at 0.5V supply.

Keywords: in-memory computing, dot-product, SRAM, multiply and accumulate, ADC, voltage-mode accumulator
Session 4: Power Management Techniques

DATE/TIME: November 5, 2019 (Tuesday) / 1:30 PM – 3:10 PM
ROOM: 7401 AB
CHAIR: Hyun-Sik Kim, KAIST
CO-CHAIR: Wanyuan Qu, Zhejiang University

A 69.3% Efficiency, 6.78-MHz Wireless Power Delivery System with 0X/1X Regulating Rectifier and Reconfigurable Power Amplifier
Jonathan Fuh, Fu-Bin Yang, Po-Hung Chen
National Chiao Tung University, Taiwan

Abstract:
In this paper, we present a 6.78-MHz high-efficiency wireless power transfer system with a reconfigurable class-D power amplifier and a 0X/1X regulating rectifier. The proposed reconfigurable power amplifier delivers 0.25X/1X output power by adjusting the power-stage configuration to improve system efficiency. To enhance the receiver efficiency, the proposed 0X/1X regulating rectifier with adaptive offset compensation achieves both voltage rectification and voltage regulation in a single conversion stage. The measurement results demonstrate a 90.1% peak receiver efficiency and a 69.3% peak system efficiency. The system provides the load circuit with 5-V regulated output and 250-mW maximum output power.

Keywords: wireless power transfer, regulating active rectifier, resonant coupling, reconfigurable power amplifier

An 80mA Capacitor-Less LDO with 6.5μA Quiescent Current and No Frequency Compensation Using Adaptive-Deadzone Ring Amplifier
Bohui Xiao2, Praveen Kumar Venkatachala2, Yang Xu4, Ahmed Elshater2, Calvin Lee2, Spencer Leuenberger3, Qadeer Ahmad Khan1, Un-Ku Moon2
1Indian Institute of Technology Madras, India; 2Oregon State University, United States; 3Skyworks Solutions Inc., United States; 4Texas Instruments, United States

Abstract:
This paper presents a capacitor-less low dropout (LDO) regulator that requires no frequency compensation, with the use of an adaptive-deadzone ring amplifier. Due to the dynamic behavior of the ring amplifier depending on the input voltage, the proposed LDO features a hybrid (digital or analog) operation and achieves both fast transient response and high output accuracy with a low quiescent current. Moreover, an adaptive deadzone biasing scheme is employed to ensure high stability for a wide range of load current operating conditions. A 1V LDO prototype with 80mA maximum load current is implemented in a 0.18μm CMOS process, consuming only a quiescent current of 6.5μA with a dropout voltage of 90mV. It achieves 172–432ns settling time for load current transitions between 1mA and 81mA. The active area...
Keywords: low dropout (LDO) regulator, capacitor-less, frequency compensation, ring amplifier, quiescent current

4 – 3 (Short Paper)  2:20 PM – 2:32 PM
A DCM ZVS Class-D Power Amplifier for Wireless Power Transfer Applications
Xinyuan Ge¹, Lin Cheng², Wing-Hung Ki¹
¹Hong Kong University of Science and Technology, Hong Kong; ²University of Science and Technology of China, China

Abstract:
A discontinuous conduction mode ZVS scheme for a class-D power amplifier (PA) for wireless power transfer is presented. The sizes of the ZVS inductor and capacitor are reduced by 7.5 and 5 times and ZVS is achieved under PA supply voltage and output current variations. The proposed class-D PA was fabricated with a 0.35 µm high-voltage CMOS process. The ZVS LC resonant tank consists of a 39 nH inductor and a 200 nF capacitor. Measurement results show that the PA delivered an output power of 7.18 W with a peak efficiency of 87.0%.

Keywords: Class-D, power amplifier, zero-voltage switching (ZVS), wireless power transfer

4 – 4 (Short Paper)  2:32 PM – 2:45 PM
Time-Based Digital LDO Regulator with Fractionally Controlled Power Transistor Strength and Fast Transient Response
Jin-Gyu Kang, Min-Gyu Jeong, Jeongpyo Park, Changsik Yoo
Hanyang University, Korea

Abstract:
The number of enabled power transistors and their ON-time of a digital low-dropout (LDO) regulator are controlled by a time-based controller. By the time-based controller consisting of two voltage-controlled oscillators (VCO) and a phase-detecting switch driver, the effective number of enabled power transistors and therefore their strength can be fractionally controlled. The transient response is greatly improved by a transient detector which selectively disables one of the two VCOs during a transient condition. At steady state, the number of switching power transistor is either zero or one, minimizing the ripple of the output voltage. Implemented in a 65 nm CMOS technology, the time-based digital LDO regulator can provide 0.5~1.1 V output from 0.9~1.2 V input. For the maximum load current of 19 mA, the peak current efficiency is 99.3 %. For both the step-up and -down changes of the load current by 3 mA, the voltage level of the output is stabilized in less than 90 ns.

Keywords: Low-dropout regulator (LDO), digital LDO, time-based control, voltage-controlled oscillator (VCO), CMOS
A Single-Inductor Triple-Output Converter with an Automatic Detection of DC or AC Energy Harvesting Source for Supplying 93% Efficiency and 0.05mV/MA Cross Regulation to Wearable Electronics

T. Nagateja¹, Shao-Qi Chen¹, Li-Cheng Chu¹, Ke-Horng Chen¹, Ying-Hsi Lin², Shian-Ru Lin², Tsung-Yen Tsai²

¹National Chiao Tung University, Taiwan; ²Realtek Semiconductor Corp, Taiwan

Abstract:
The proposed single-inductor triple-output (SITO) converter can accept both DC battery voltage and AC energy harvesting voltage to provide a triple step up and down outputs. Storing the energy to the H-bridge capacitor first and pumping it later can ensure a continuous inductor current for reducing the output voltage ripple by 67%. Due to the H-bridge, the inductor current value is reduced to 1/5X to achieve high efficiency of 93% under the current loading of 120mA. Moreover, the proposed PWM and the adaptive on-time hybrid controller uses different modulation methods in a single controller to meet the requirements of different multiple outputs.

Keywords: single-inductor triple-output (SITO) converter, pulse width modulation (PWM), adaptive on-time (AOT)
A 0.7mm² 8.54mW FocusNet Display LSI for Power Reduction on OLED Smart-Phones
Tsu-Ming Liu, Chang-Hung Tsai, Shawn Shih, Chih-Kai Chang, Jia-Ying Lin, Wayne Hsieh, Yung-Chang Chang, Chi-Cheng Ju
MediaTek Inc., Taiwan

Abstract:
The first-reported ConvNet-Focus display LSI integrating a 22-layer neural-network and supporting color, contrast and sharpness enhancement is fabricated in a 10nm process. A ConvNet-Focus network model extracts the human’s focus region applying a tone mapping curve so as to decrease the pixel luminance, leading to 26.86mA of current saving on OLED smart-phone. Moreover, input channel reduction and layer merging approaches reduce ConvNet-Focus complexity by 69%. Operated at 0.9V and 205MHz, the proposed deep-learning (DL)-assisted FHD display LSI occupies 0.7mm² and consumes 8.54mW of power dissipation.

Keywords: tone mapping, deep-learning, display, OLED

A 47.4µJ/epoch Trainable Deep Convolutional Neural Network Accelerator for In-Situ Personalization on Smart Devices
Seungkyu Choi, Jaehyeong Sim, Myeonggu Kang, Yeongjae Choi, Hyeonuk Kim, Lee-Sup Kim
KAIST, Korea

Abstract:
A scalable deep learning accelerator supporting both inference and training is implemented for device personalization of deep convolutional neural networks. It consists of three processor cores operating with distinct energy-efficient dataflow for different types of computation in CNN training. Two cores conduct forward and backward propagation in convolutional layers and utilize a masking scheme to reduce 88.3% of intermediate data to store for training. The third core executes weight update process in convolutional layers and inner product computation in fully connected layers with a novel large window dataflow. The system enables 8-bit fixed point datapath with lossless training and consumes 47.4µJ/epoch for a customized deep CNN model.

Keywords: Processor, ASIC, Accelerator, Deep learning, Convolutional neural networks
A Sparse-Adaptive CNN Processor with Area/Performance Balanced N-Way Set-Associate Pe Arrays Assisted by a Collision-Aware Scheduler

Zhe Yuan\textsuperscript{2}, Jingyu Wang\textsuperscript{2}, Yixiong Yang\textsuperscript{2}, Jinshan Yue\textsuperscript{2}, Zhibo Wang\textsuperscript{2}, Xiaoyu Feng\textsuperscript{2}, Yangzhi Wang\textsuperscript{1}, Xueqing Li\textsuperscript{2}, Huazhong Yang\textsuperscript{2}, Yongpan Liu\textsuperscript{2}

\textsuperscript{1}Northeastern University, United States; \textsuperscript{2}Tsinghua University, China

Abstract:
Convolutional Neural Networks give heavy storage and computation burdens to accelerators, whose energy efficiency can be improved by leveraging their sparsity. However, using sparsity in networks will introduce large overhead especially when networks have various sparse situations and multiple quantization bit. This work firstly proposes an area/performance balanced chip with simultaneously sparsity/quantization adaptive capability, enabled by multi-sparsity and multi-quantization compatible storage and computation circuits. Furthermore, N-way set-associate PE architecture is explored to trade off its performance and area with the collision-aware hardware scheduler when processing sparse networks. This chip achieves 4.64 TOPS/W energy efficiency on Alexnet, 1.69x better than the state-of-the-art sparse processors, along with 19.4% PE area reduction.

Keywords: Neural Network, Accelerator, Sparsity, Quantization

A 2.25 TOPS/W Fully-Integrated Deep CNN Learning Processor with On-Chip Training

Cheng-Hsun Lu, Yi-Chung Wu, Chia-Hsiang Yang

National Taiwan University, Taiwan

Abstract:
This paper presents the an energy-efficient deep learning processor that supports both inference and training for the entire convolutional neural network (CNN) with any size. Filter re-arrangement and operations reformulation are utilized to reduce the latency by 88%. Integration of fixed-point and floating-point operators reduces the area of the multiplier by 56.8%. A unified processing element (PE) unit has 33% less area. In the low-precision mode, clock gating and data gating are employed to reduce the power by 62%. Maxpooling and ReLU modules are co-designed to reduce the memory requirement by 75%. The softmax function is modified to reduce the area by 78%. Fabricated in 40nm, the chip achieves a competitive energy efficiency in inference as the state-of-the-art designs. It also achieves a 2x105 times higher energy efficiency in training compared to a CPU.

Keywords: Deep learning, convolutional neural network, specialized processor, CMOS digital integrated circuits
A Ka-Band CMOS Phase-Inverting Amplifier with 0.6 dB Gain Error and 2.5° Phase Error
Chenyu Xu, Dixian Zhao
Southeast University, China

This paper demonstrates the design of a Ka-band 0°/180° phase-inverting amplifier (PIA) based on a 3-port transformer in 65-nm CMOS technology. Cascode topology with common-gate (CG) switch is employed to increase the reverse isolation and gain. Layout optimization techniques including double parallel inductors and self-resonant capacitor are used to improve the balance performance. The proposed PIA achieves 10.4 dB gain at 26.5 GHz with 3-dB bandwidth of over 6 GHz (i.e., 24-30 GHz). The maximum measured gain and phase errors are 0.6 dB and 2.5°, respectively. The DC power consumption is only 2.4 mW with 1-V supply.

Keywords: phase-inverting amplifier (PIA), millimeter-wave, double parallel inductors, self-resonant capacitor, CMOS

A High-Performance Low Complexity All-Digital Fractional Clock Multiplier
Nahla Abou-El-Kheir², Ralph Mason¹, Mingze Li¹, Mustapha Yagoub²
¹Carleton university, Canada; ²university of Ottawa, Canada

Abstract:
A fractional Injection Locked Clock Multiplier (ILCM) based on an injection locked Digitally Controlled Ring Oscillator (DCRO) is proposed in this work. Process Voltage Temperature (PVT) calibration was performed using a replica oscillator and a high speed digital counter. The proposed design was fully synthesized and designed in a TSMC 65nm GP CMOS process with no analog or RF enhancements. The measured phase noise (1 MHz offset) and RMS jitter (1 kHz to 30 MHz) for 3.125×fref injection locking were found to be -126 dBC/Hz and 251fs, respectively. The ILCM consumes 13.25 mW and has a fraction resolution of fref/32.

Keywords: ILCM, DCO, fractional, PVT calibration, ring oscillator, fully synthesizable

A DC-43.5 GHz CMOS Switched-Type Attenuator with Capacitive Compensation Technique
Peng Gu, Dixian Zhao
Southeast University, China

Abstract:
This paper presents an ultra-broadband 5-bit switched-type attenuator (STA). The resistor values of the five attenuation cells are optimized to ensure accurate amplitude tuning. Capacitive compensation technique is adopted to reduce phase error and enhance the bandwidth. Fabricated in 65-nm CMOS technology, the 5-bit STA occupies a core chip area of 0.036 mm$^2$. It exhibits ultra-broadband (i.e., DC to 43.5 GHz) operation with 15.5-dB amplitude tuning range and 0.5-dB tuning step. The insertion loss of the reference state is 1.5 – 5.3 dB from DC to 43.5 GHz. The RMS amplitude error and phase error are < 0.19 dB and < 3.1° over the whole measured band.

Keywords: phased-array system, amplitude tuning, switched-type attenuator, capacitive compensation, CMOS

6 – 4 (Short Paper)  2:32 PM – 2:45 PM

A 28-GHz Compact SPDT Switch Using LC-Based Spiral Transmission Lines in 65-nm CMOS
Xiangyu Meng$^2$, Zhenpeng Zheng$^2$, Jiaqi Zhang$^2$, C. Patrick Yue$^1$
$^1$Hong Kong University of Science and Technology, China; $^2$Sun Yat-sen University, China

Abstract:
A novel LC-based spiral transmission line consisting of only one three-turn inductor and two capacitors is proposed for the first time. Based on this structure, the function of the quarter-wavelength transmission line can be realized with smaller area and less insertion loss compared with conventional micro-strip transmission lines. By using the LC-based spiral transmission line, a compact Single Pole Double Throw (SPDT) switch is implemented in 65-nm CMOS. The SPDT switch occupies only 0.028 mm$^2$ area with measured 1.3-dB insertion loss and 24-dB isolation at 28 GHz.

Keywords: SPDT, transmission line, millimeter-wave, CMOS

6 – 5  2:45 PM – 3:10 PM

A 20-GHz Ultra-Low-Power LNA Using gm-Boosted and Current-Reuse Techniques in 65-nm CMOS for Satellite Communication Terminals
Jiajun Zhang, Dixian Zhao
Southeast University, China

Abstract:
A 20-GHz low-power low-noise amplifier (LNA) in 65-nm CMOS is presented. The LNA is cascaded with a single-ended gm-boosted common-gate (CG) stage and a differential neutralized common-source (CS) stage. The current-reuse technique is employed to save the power consumption. The LNA achieves a measured power gain of 14.9 dB at 21 GHz with a – 3-dB bandwidth of 4.8 GHz. The lowest noise figure (NF) is 3.3 dB at 20 GHz. The LNA consumes
1.9 mW from a 1-V supply, with a chip area of 600 μm × 700 μm.

Keywords: CMOS, current-reuse, K-band, low-noise amplifier (LNA), low-power
A 4-GHz Sub-Harmonically Injection-Locked Phase-Locked Loop with Self-Calibrated Injection Timing and Pulsewidth

Xuefan Jin, Dong-Seok Kang, Youngjun Ko, Kee-Won Kwon, Jung-Hoon Chun
Sungkyunkwan University, China; Sungkyunkwan University, Korea

Abstract:
A 4-GHz sub-harmonically injection-locked phase locked loop (ILPLL) with on-chip calibration is presented. The injection timing and pulsewidth of the injected pulse are self-calibrated to achieve a low phase noise. The phase noise of the proposed ILPLL was -110.1 dBc/Hz at 1-MHz offset frequency, while that of the conventional PLL was -104.8 dBc/Hz. The measured reference spur was also reduced from -44.36 dBc to -52.87 dBc with the proposed calibration technique. Fabricated in a 28-nm CMOS process, the proposed ILPLL occupies 0.09 mm². Operating at 4 GHz, it consumes 11.4 mW from a 1.0-V power supply.

Keywords: Ring oscillator, phase-locked loop (PLL), injection- locked PLL (ILPLL), injection-locked ring oscillator (ILRO), self-calibrated

A 9.4MHz-to-2.4GHz Jitter-Power Reconfigurable Fractional-N Ring PLL for Multi-Standard Applications in 7nm FinFET CMOS Technology

Sangdon Jung, Jaehong Jung, Byungki Han, Seunghyun Oh, Jongwoo Lee
Samsung Electronics, Korea

Abstract:
This paper proposes a ring-VCO-based fractional-N PLL with a noise-power reconfigurable ring-VCO and a self-chopped reference frequency doubler for multi-standard applications. To cover the various specifications of SoC chips, the jitter and power of the proposed PLL can be tuned through the RC adjustments of the ring-VCO. Moreover, the reference frequency doubler provides 6 dB improvements on in-band noise and DSM quantization noise. In addition, this PLL also guarantees a wide frequency range from 9.4 MHz to 2.4 GHz, and maintains optimum loop bandwidth across process, supply voltage, and temperature variations through an adaptive bandwidth technique. The measured integrated RMS jitter of this 7nm FinFET PLL is 6.2 ps consuming 6.0 mW which is -216.4 FoM for the low jitter specification, and 13.2 ps consuming 2.0 mW which results in an efficiency of 0.85 mW/GHz for low power specification.

Keywords: Fractional-N PLL, phase noise, reconfiguration, ring-VCO, doubler
A 2.4-GHz 500-μW 370-Fs rms Integrated Jitter Sub-Sampling Sub-Harmonically Injection-Locked PLL in 90-nm CMOS
Chun Yu Lin, Yu Ting Hung, Tsung Hsien Lin
National Taiwan University, Taiwan

Abstract:
This paper proposes a sub-sampling (SS) sub-harmonically injection-locked (SI) PLL. Both the SS and SI techniques are incorporated to realize a low-jitter low-power PLL. To ensure both techniques operate coherently, the injection timing of the SI path is calibrated through the assist of the SS loop. Fabricated in a 90-nm CMOS, the proposed 2.4-GHz PLL consumes only 500 μW from a 1-V supply. With a 40-MHz reference frequency, this SS-SIPLL achieves 370-fs rms integrated jitter (10 kHz to 30 MHz); the FOM is -251.6 dB.

Keywords: sub-sampling PLL, injection-locked PLL, gating operation

A Sub-Sampling PLL with Robust Operation Under Supply Interference and Short Re-Locking Time
Yuan Cheng Qian, Yen-Yu Chao, Shen-Iuan Liu
National Taiwan University, China; National Taiwan University, Taiwan

Abstract:
A sub-sampling phase-locked loop (SSPLL) is presented to tolerate the supply interference and have a short re-locking time when divider ratio is switched. A sampling phase detector, a voltage-to-current converter and a mini-dead zone creator are presented. The low in-band phase noise of the proposed SSPLL is kept and the power penalty is low.

Keywords: sub-sampling PLL, Robust PLL, short re-locking time
Session 8: Panel Discussion
DATE/TIME: November 5, 2019 (Tuesday) / 3:40 PM – 5:20 PM
ROOM: 7402-7403 & 7502-7503
MODERATOR: Noriyuki Miura, Kobe University

Are Analog and Mixed Mode Circuits the future solution of AI SoCs?

Abstract
DNN looks mature already, and Neuromorphic and Spike Neural Network are regarded as the next research area. The current AI SoCs are based on Digital DNN circuits with the limitations from the Von Neumann architecture. Analog/Mixed Mode circuits may implement Neuromorphic SoCs and Spike Neural Network overcoming the Von Neumann bottleneck. Is it true? and if it is, how we can make it?

• Just ADC/DAC are enough to process AI operations
• Are Mixed Mode MACs better than Digital MACs?
• DRAM and SRAM can be the Processing Elements.
• Non-Volatile Memory is essential to implement Neuromorphic/SNN
• What kind of circuits do you need for Spike Neural Network?
• Neuromorphic AI and Mixed Mode Circuits.

Organizer/Co-organizer: Woogeun Rhee, Tsinghua University, China, Jerald Yoo, National University of Singapore, Singapore, Noriyuki Miura, Kobe University, Japan

Moderator: Noriyuki Miura, Kobe University, Japan

Panelists / Position:
1) Mixed Mode AI Trends Overview: Jason Lee (UNIST)
2) ADC and AI: Vanessa Chen (Carnegie Mellon University)
3) Mixed Mode MAC: SeungTak Ryu (KAIST)
4) Memory Based Analog AI: ShouYi Yin (Tsinghua University)
5) Non-Volatile Memory and Analog AI: Yongpan Liu (Tsinghua University)
6) Spike Neural Network: Samuel Tang (National Tsinghua University)
7) Neuromorphic: Hiromitsu Awano (Osaka University)
Plenary Talk 3  
TITLE: AI and IoT for Social Value Creation  
DATE / TIME: November 6, 2019 (Wednesday) / 8:30 AM – 9:15 AM  
SPEAKER: Dr. Yasunori Mochizuki, NEC Fellow NEC Corporation

Abstract:
The features of AI and IoT technologies leading to the realization of next smart cities/smart communities are discussed. The AI topics included are person identification AI for biometrics, white-box/explainable AI for value chain innovation, whose use cases reveal how these technologies are contributing to the broader range of new social values. IoT system also has significant implications in realizing the next smart society. Here, interoperability and openness are becoming increasingly important for scalability and cross-domain data utilization of solutions, in quest to the realization of citizen-centric and economically sustainable, thereby future-proof smart cities.

Biography:
Dr. Yasunori Mochizuki is an NEC Fellow since April, 2019 and is engaged in Digital Transformation and IoT eco-systems strategy for Smart Cities. Previously, he was a Senior Vice President responsible for the NEC’s corporate technology strategy including R&D roadmap and open innovations. He has 30+ years of career as a research scientist and then as a general manager of research departments and his technical expertise covers a broad area including AI-oriented computer science, ICT systems, integrated devices and solid-state physics. Dr. Yasunori Mochizuki is also active in NPO as well as policy making activities related to digital innovation for smart cities: he is a Fellow for Smart City Project of World Economic Forum’s Center for the Forth Industrial Revolution and also is a board member of FIWARE Foundation since March, 2017 representing NEC.
Dr. Mochizuki has published more than 80 papers in technical journals and international conferences. He is the Fellow of Japan Society of Applied Physics. He is a JSAP Executive Committee member of Symposia on VLSI Technology and Circuits, and is also a research advisor to Institute of Industrial Science, University of Tokyo. Dr. Mochizuki received his BS, MS and PhD in Electronics Engineering from University of Tokyo.
Abstract:
This paper highlights a wide range of (sub)-mm-Wave system-on-chip (SoC) applications from space exploration to contactless connectivity. Passive and active SoCs developed at UCLA and NCTU, including heterodyne-radiometer, spectrometer processor, and multiband radio/radars, will be exemplified as cost/weight/energy-effective ways to explore astrophysics and earth/planetary sciences. Multi-Giga-bit/sec contactless connectors based on mm-Wave radios have also been successfully developed and commercialized to replace high-performance mechanical connectors/cables for smartphones, electrical cars, and data centers. Techniques to augment range and bandwidth efficiency according to PAM-4 modulations and flexible plastic waveguide are also reviewed with design and test results.

Biography:
Dr. Mau-Chung Frank Chang is the President of National Chiao Tung University, Hsinchu, Taiwan. He is also the Wintek Chair Professor of Electrical Engineering at UCLA. Prior to joining UCLA in 1997, Dr. Chang was the Assistant Director and Department Manager of the High Speed Electronics Laboratory at Rockwell Science Center, Thousand Oaks, California. Throughout his career, his research has primarily focused on developing high-speed semiconductor devices and high frequency integrated circuits for radio, radar and imaging system-on-chip applications up to terahertz frequency regime.

He is a Member of the US National Academy of Engineering, a Fellow of National Academy of Inventors, an Academician of Academia Sinica, Taiwan, and a Fellow of IEEE. He was honored with the IEEE David Sarnoff Award in 2006 for developing and commercializing GaAs HBT and BiFET power amplifiers for high efficiency and high linearity smart-phones throughout the past 2.5 decades. He has also received numerous awards including Rockwell's Leonardo Da Vinci Award (1992), IEEE Davis Sarnoff award (2006), Pan Wen Yuan Foundation Award (2008), John J. Guerrera Engineering Educator of the Year Award (Engineers’ Council, 2014), IET’s J.J. Thomson Medal for Achievement in Electronics (2017), and IEEE Eta Kappa Nu (HKN) Vladimir Karapetoff Outstanding Technical Achievement Award (2018).
An Energy-Efficient BJT-Based Temperature-to-Digital Converter with ±0.13°C (3σ) Inaccuracy from -40 to 125°C
Rushil Kishore Kumar, Hui Jiang, Kofi Makinwa
Delft University of Technology, Netherlands

Abstract:
This paper describes an energy-efficient BJT-based temperature-to-digital converter (TDC) with a state-of-the-art resolution FoM (RFoM) of 5.4pJ·K^2. It consists of a BJT front-end, a capacitively-coupled instrumentation amplifier (CCIA) and a 2nd-order continuous-time (CT) ΔΣADC. The front-end and the CCIA employ bitstream-controlled dynamic element matching (DEM) and chopping to mitigate mismatch and 1/f noise without incurring quantization noise fold-back. The sensor achieves ±0.13°C (3σ) inaccuracy from -40 to 125°C and has a supply sensitivity of 8.2mK/V.

Keywords: CCIA, CTΔΣADC, BJT Temperature Sensor, DEM, Chopping, Quantization Noise Fold-Back

A 16.1-b ENOB 0.064mm² Compact Highly-Digital Closed-Loop Single-VCO-Based 1-1 Smash Resistance-to-Digital Converter in 180nm CMOS
Elisa Sacco¹, Johan Vergauwen², Georges Gielen¹
¹Katholieke Universiteit Leuven, Belgium; ²Melexis Technologies, Belgium

Abstract:
This paper presents a novel highly-digital area- and energy-efficient closed-loop time-based CMOS single-ended resistive sensor-to-digital readout circuit. It achieves a high resolution of 16.1 bits utilizing a time-based implementation in an extremely small area of only 0.064mm². It employs a single VCO and a digital feedback loop for the read-out of an external single-ended resistive sensor such as a NTC thermistor. In addition to inherent 1st-order quantization noise shaping due to the oscillator, a second loop in SMASH configuration creates 2nd-order noise shaping. The fabricated prototype in a 180nm CMOS process achieves 16.1 bit of resolution for 1ms conversion time and consumes 171μW, resulting in a 2.4pJ/c.s. FOMW, which is excellent for a resistive sensor interface. Thanks to the closed-loop architecture, it also achieves more than 13 bits of linearity.

Keywords: resistive sensor readout circuit, VCO-based, time-based, ΔΣ modulator, noise shaping
A Low-Noise Sub-Bandgap Reference with a ±0.64% Untrimmed Precision in 16nm FinFET
Matthias Eberlein, Harald Pretl

Abstract:
This paper presents a new concept for sub-bandgap circuits, based on direct generation of PTAT current with larger and adjustable temperature coefficient. The reference voltage is generated inside the feedback loop, which facilitates good supply rejection, low-noise and high precision performance. A 3σ-spread of only ±0.64% across split-lots was observed in a 16nm FinFET process on 4400µm², without trimming or any switching techniques. By using NPN bipolar devices, noise levels of ~130nV/sqrt(Hz) at 1kHz can be achieved at 125µA power drain. Different configurations are explained, which allow flexible reference levels or very low supply voltages of < 0.85V.

Keywords: bandgap, voltage reference, NPN bipolar, low-noise
Abstract:
This paper presents a multi-slice VCO-based quantizer (MSVQ) for high-resolution power supply noise analysis. To relax the trade-off between accuracy and measurement time, a multi-slice quantizer at a relatively higher sampling rate is proposed, and the auto-covariance replaces the autocorrelation to obtain PSD while immunes the spurs introduced by the quantizers itself and further reduces noise floor. 0.11 (mV)^2/sqrt(MHz) noise floor is achieved with a significantly reduced measurement time of 336s.

Keywords: power supply noise, spectrum analyzer, VCO quantizer

A 265µW Continuous-Time 1-2 MASH ADC Achieving 100.6 dB SNDR in a 24 kHz Bandwidth
Sujith Billa, Suhas Dixit, Shanthi Pavan
Indian Institute of Technology Madras, India

Abstract:
We present a high-performance audio CTDSM that uses an FIR-filtered 1-2 MASH architecture. The modulator uses a singe-bit first-order input stage that achieves a maximum stable amplitude close to full-scale in spite of using a 1-bit quantizer. We show that FIR feedback can be used to advantage in a MASH converter by effectively filtering the first-stage error that is coupled to the second stage. Our design achieves 100.6,db peak SNDR in a 24,kHz bandwidth, resulting in a Schreier FoM in excess of 180,db.

Keywords: data converter, sigma delta, MASH, continuous-time
11 – 1 10:30 AM – 10:55 AM
Drop-in Energy-Performance Range Extension in Microcontrollers Beyond VDD Scaling
Saurabh Jain, Longyang Lin, Massimo Alioto
National University of Singapore, Singapore

Abstract:
This work introduces reconfigurable thread count augmentation for existing microcontroller architectures, and row aggregation for their dedicated SRAM memory, to extend their energy-performance tradeoff beyond traditional voltage scaling, while at minimal design effort (“drop-in”). The proposed techniques are architecture-agnostic as the added reconfigure-ability does not modify the original instruction execution down to the cycle level. A 40nm ARM Cortex-M0 testchip shows 1.8X (1.4X) core (memory) performance boost beyond a baseline at nominal voltage, 1.4X lower minimum energy point at only 16% (4%) area (timing) overhead, and lowest energy/cycle to date.

Keywords: Energy efficiency, beyond-voltage scaling energy-performance tradeoff, processor, microarchitecture, SRAM

11 – 2 10:55 AM – 11:20 AM
A 28nm Fully Digital Voltage Monitor with 16.5uV/°C Accuracy and 0.8mV Quantized Error from -40 to 160°C for ISO26262 ASIL-D Capable MCU
Toshifumi Uemura, Yuko Kitaji, Kazuki Fukuoka
Renesas Electronics Corporation, Japan

Abstract:
A fully digital voltage monitoring system has been developed for automotive ISO26262 ASIL-D capable MCUs to detect internal under-voltage fault at IR-drop hotspots and to mitigate large Vmin margin due to voltage detection variation. Proposed oscillators employing temperature coefficient tuners enable digitized voltage detection with small temperature drift and quantized error. A digital voltage monitor fabricated in 28nm shows temperature drift of 16.5 uV/°C and 0.8mV quantized error. The total voltage detection variation of 4.1mV is the smallest and the temperature range from -40 to 160°C is the largest compared with previous works.

Keywords: digital voltage monitor, reference voltage less

11 – 3 (Short Paper) 11:20 AM – 11:32 AM
HyCUBE: a 0.9V 26.4 MOPS/mW, 290 pJ/op, Power Efficient Accelerator for IoT Applications
Bo Wang, Manupa Karunarathne, Aditi Kulkarni, Tulika Mitra, Li-Shiuan Peh
National University of Singapore, Singapore

Abstract:
IoT devices use ultra-low-power micro-controllers that cannot handle the performance demands of emerging compute-intensive applications. Accelerators can be added to improve system power-performance efficiency. We present HyCUBE, a Coarse-Grained Reconfigurable Array (CGRA) accelerator chip that realizes 127X improvement in power efficiency compared to TI Sensortag IoT platform. HyCUBE has a bufferless Network-on-Chip (NoC), enabling single-cycle data traversal to boost throughput and a software-scheduled architecture, automatically extracting application parallelism. Our 40nm test chip delivers peak efficiency of 26.4 MOPS/mW with 290 pJ/operation, realizing a power efficiency improvement of 28.6X and 26.5X compared to Xilinx Zynq FPGA and ARM Cortex-A7 core.

Keywords: power efficient, IoT, accelerator

11 – 4 (Short Paper)  11:32 AM – 11:45 AM

A 54% Power-Saving Static Fully-Interruptible Single-Phase-Clocked Shared-Keeper Flip-Flop in 14nm CMOS
Amit Agarwal, Steven Hsu, Monodeep Kar, Mark Anders, Himanshu Kaul, Raghavan Kumar, Vikram Suresh, Sanu Mathew, Ram Krishnamurthy, Vivek De
Intel Corporation, United States

Abstract:
A low clock power, static, fully-interruptible, single-phase-clocked, shared-keeper flip-flop without local clock inverters and no write-back failure reduces the clock transistor count to 6 instead of 12 in conventional transmission-gate flip-flop, achieving 54% reduction in total cell level power and 100mV improved VMIN. An experimental microcontroller with shared-keeper sequentials, fabricated in 14nm CMOS, shows 6.5% lower measured chip level power at iso-frequency compared to the previously published single-phase-clocked AOI sequentials at 0.75V, 25°C

Keywords: low-clock-power, flip-flop, latch, integrated clock gate

11 – 5  11:45 AM – 12:10 PM

0.54 pJ/bit, 15Mb/s True Random Number Generator Using Probabilistic Delay Cell for Edge Computing Applications
Fei Li, Ming Ming Wong, Aarthy Mani, Vishnu Paramasivam, Anh Tuan Do
Agency for Science, Technology and Research, Singapore

Abstract:
This paper presents a true random number generator utilizing the probabilistic delay of the cross-coupled latch during start up as an entropy source. The start-up signal is used as a slow and jittered clock to sample a fast ring oscillator to harvest random bit stream. The tunable
jitter delay range and all-digital design ensures high quality random bits generation across a wide range of supply voltages. The test chip consumes 0.54 pJ/bit with a bit rate of 15Mb/s at 0.5 V supply voltage while occupying only 18% area of the state of the art. The design's compact area, simple interface; and high energy efficiency make it well suited choice edge computing applications.

Keywords: True Random Number Generator, Edge computing, CMOS, Low-power

11 – 6

12:10 PM – 12:35 PM

A Smart Hardware Security Engine Combining Entropy Sources of ECG, HRV and SRAM PUF for Authentication and Secret Key Generation
S. Cherupally¹, S. Yin¹, D. Kadetotad¹, C. Bae², S. Kim², J. Seo¹
¹Arizona State University, United States; ²Samsung Advanced Institute of Technology, Korea

Abstract:
We present a smart hardware security engine that combines three different sources of entropy, electrocardiogram (ECG), heart rate variability (HRV) and SRAM-based physical unclonable function (PUF), to perform real-time authentication and generate unique and random signatures. Such hybrid signatures vary person-to-person, device-to-device, and over time, and hence can be used for personal device authentication as well as secret random key generation, significantly reducing the scope of an attack. The prototype chip fabricated in 65nm LP CMOS consumes 4.04 µW at 0.6 V for real-time authentication. Compared to ECG-only authentication, the equal error rate of multi-source authentication is reduced by 18.9X down to 0.09% for an in-house database. 256-bit random numbers generated by optimally combining ECG, HRV and PUF values pass NIST randomness tests with 100% pass rate.

Keywords: Hardware security, PUF, ECG, authentication, random number generation
A Packaged Fully Digital 390GHz Harmonic Outphasing Transmitter in 28nm CMOS
Alexander Standaert, Patrick Reynaert
Katholieke Universiteit Leuven, Belgium

Abstract:
This paper presents a fully digital 390 GHz harmonic outphasing transmitter in a 28nm CMOS technology. The proposed architecture features the combination of phase predistortion and outphasing at the third harmonic enabling higher-order non constant envelope modulation schemes which is inherently difficult in multiplier-last architectures used in conventional THz data transmitters. The transmitter includes a 5-bit outphasing symbol generator at 15 GHz which can generate the necessary symbols for a variety of modulation schemes from OOK to STAR16 QAM. The transmitter is fully packaged with a micromachined waveguide flange such that it provides a standard waveguide output. It produces a peak output power of −16 dBm with a 3 dB IF bandwidth of 16.5 GHz and has a maximum measured data rate of 6 Gbps.

Keywords: THz, Outphasing, Transmitter

A Fully Integrated 27.5-30.5 GHz 8-Element Phased-Array Transmit Front-End Module in 65 nm CMOS
An'An Li\textsuperscript{1}, Yingtao Ding\textsuperscript{1}, Zipeng Chen\textsuperscript{2}, Wei Wang\textsuperscript{2}, Sijia Jiang\textsuperscript{2}, Shiyan Sun\textsuperscript{1}, Zhiming Chen\textsuperscript{1}, Baoyong Chi\textsuperscript{2}
\textsuperscript{1}Beijing Institute of Technology, China; \textsuperscript{2}Tsinghua University, China

Abstract:
A fully integrated 27.5-30.5 GHz 8-element phased-array transmit front-end module in 65 nm CMOS is presented. A 5-bit digital attenuator with amplitude and phase calibration is presented to provide 15.5 dB attenuation with 0.5 dB step. A 180° RTPS, along with an 0/180° switching amplifier is proposed to realize 360° phase shifting with 5.625° step. Amplifiers adopt wideband inter-stage matching technique to ensure bandwidth. The measurements show that the module achieves about 36 dB gain, 12.71 dBm OP1dB, 2.61° RMS phase error from the phase shifter and 0.26 dB RMS amplitude error from the attenuator, which is competitive compared with the-state-of-the-art.

Keywords: Phased-array, phase shifter, attenuator, power amplifier, CMOS, transmit front-end module
A 2Mbps Sub-100µW Crystal-Less RF Transmitter with Energy Harvesting for Multi-Channel Neural Signal Acquisition
Heng Huang, Milin Zhang, Guolin Li, Zhihua Wang
Tsinghua University, China

Abstract:
This paper presents a 427MHz OOK transmitter with energy harvesting for multi-channel neural acquisition. A power efficient OOK modulator is proposed integrated a 3-input AND gate array to drive the power transistors. It reduce driving capability of the VCO output A 9-stage VCO is designed with PLL and edge-combining technology. A crystal based 6.78MHz oscillator is combined with the coil to power up the transmitter and generate a reference frequency resulting a crystal-less transmitter design. the power consumption is 96 uW with a -19dBm output. A 48pJ/bit efficiency is achieved under a data rate of 2Mbps.

Keywords: Energy havering, wireless power transmission, transmitter, neural signal acquisition, ultra-low-power, ring oscillator, edge-combining, phase locked loop

Direct-Conversion Receiver Front-End for 180 GHz with 80 GHz Bandwidth in 130 nm SiGe
Paul Stärke, Andres Seidel, Corrado Car, Frank Ellinger
Technische Universität Dresden, Germany

Abstract:
An integrated direct-conversion receiver for 180GHz with 80GHz bandwidth. It consists of a mixer with IF buffer, LO driver and LNA. The conversion gain is 14dB with 12dB NF. The LO power is -10dBm and the RF 1-dB compression point occurs at -15dBm. The LO driver allows a carrier range of 160 to 200GHz. The power consumption is 100mW and the chip occupies 0.75mm². It is fabricated in 130nm SiGe BiCMOS. This circuit offers one of the highest RF bandwidth of any receiver with fixed carrier.

Keywords: receiver, direct conversion, mixer, amplifier, balun, communication system, G band, mm-wave, SiGe, BiCMOS

A Blocker-Tolerant Direct Sampling Receiver for Wireless Multi-Channel Communication in 14nm FinFET CMOS
Barosaim Sung, Chilun Lo, Jaehoon Lee, Sangdon Jung, Seungjin Kim, Jaehong Jung, Seungyong Bae, Youngsea Cho, Yong Lim, Dooseok Choi, Myeongcheol Shin, Soonwoo Choi, Byungki Han, Seunghyun Oh, Jongwoo Lee
This paper presents a low power and area efficient wireless direct sampling receiver (DSR) implemented in 14nm FinFET process for frequency modulation (FM) receiver. By employing digital mixer for channel selection, the inductor based local oscillator can be removed, and I/Q matching requirements in analog front-end are vastly relaxed. Implemented in a 14nm FinFET process, the proposed FM-DSR with FPGA based demodulation achieves 31 dB SNR with $-90$ dBm sensitivity level and 71 dB SNR with $-47$ dBm input power while consuming 11.74 mW.

Keywords: Frequency modulation, receiver, software radio

A 2.4 GHz highly power efficient receiver front-end for Bluetooth Low Energy (BLE) is presented in this paper. Thanks to the extensive current reuse scheme combined with the passive source-boosting topology and exploiting forward back gate biasing (FBB) of active devices, the low-noise transconductance amplifier (LNTA) input impedance is matched to 50Ω with 18 times less current compared to a single common-gate (CG) LNTA. Moreover, a high swing Class-C VCO operating at the twice the desired frequency drives the frequency divider by 2 to create 4 phases with 25% duty cycle. Implemented in 22 nm FD-SOI technology, the proposed receiver front-end consumes only 330 μW from 0.65 V and occupies an active area of 0.15 mm². The measured conversion gain and NF are 32.3 dB and 11.5 dB respectively. The proposed receiver consumes the least power among all previous published papers while its performance is largely superior to the requirement of intended applications.

Keywords: ultra low-power (ULP), current reuse, gm-boosting, Internet of thing (IoT), LNTA, Class-C VCO
A 4-Mbps 41-pJ/bit On-off Keying Transceiver for Body-Channel Communication with Enhanced Auto Loss Compensation Technique

Jian Zhao¹, Jingna Mao², Wenyu Sun³, Yuxuan Huang³, Yixiong Yang³, Huazhong Yang³, Yongpan Liu³
¹Chinese Academy of Sciences, China; ²Shanghai Jiao Tong University, China; ³Tsinghua University, China

Abstract:
This paper presents a body-channel communication (BCC) transceiver for wireless body sensor network applications. The transceiver employs on-off keying (OOK) modulation and operates in the quasi-static band. It achieves high energy efficiency and stability through two innovative methods: 1) an auto-loss compensation (ALC) technique attenuates the time-variant path loss in the wearable scenario; 2) a capacitive interface in the receiver strengthens the path loss compensation. The transceiver is designed and fabricated in 180-nm CMOS process, it achieves 4-Mbps data rate with a 41-pJ/bit efficiency over 1.5-m distance.

Keywords: Wireless-body-area network, body-channel communication, auto-loss compensation, transceiver, energy efficiency

A Battery-Less 31 mW HBC Receiver with RF Energy Harvester for Implantable Devices

Jihee Lee, Jaeeun Jang, Jaehyuk Lee, Hoi-Jun Yoo
KAIST, Korea

Abstract:
A power-efficient human body channel (HBC) RX IC which operates without external battery is implemented in 65 nm CMOS mixed mode process with 0.6 V supply voltage. The HBC RX IC is designed to receive intermittent data from an external device while generating power by itself. The HBC RX IC integrates an ambient RF energy harvester (EH), a wireless power transfer (WPT)-based wake-up receiver (WuRX), and a low-power main HBC RX.

Keywords: battery-less, body area network, body channel communication, energy harvester, human body communication, implantable device, low power, receiver, wake
A Piezoelectric Energy Harvesting Interface for Irregular High Voltage Input with Partial Electric Charge Extraction with 3.9× Extraction Improvement
Muhammad Bilawal Khan, Hassan Saif, Yoonmyung Lee
Sungkyunkwan University, Korea

Abstract:
A novel energy harvesting technique for piezoelectric transducers (PZTs) is proposed to enable energy harvesting from irregular high voltage inputs. With the proposed partial electrical charge extraction (PECE) scheme, a small portion of the charges generated by the PZT is repeatedly transferred to the battery until the input excitation is finished. With PECE, the PZT output voltage is automatically regulated at the maximum voltage level allowed by technology (VMAX) while maximizing energy extraction from the PZT. This allows energy harvesting from irregular PZT excitations that can generate open circuit voltage (VOC) higher than VMAX. The measurement results with a test chip fabricated in 350nm process show that the proposed harvester successfully harvests energy from the excitation with VOC of up to 60V, higher than VMAX of 30V, with up to 3.9× improvement compared with a conventional full bridge rectifier (FBR).

Keywords: piezoelectric energy harvester, PZT, PECE, partial electric charge extraction, partial harvesting, wakeup controller

13 – 4 11:45 AM – 12:10 AM

A 100-pA Adaptive-FOCV MPPT Circuit with >99.6% Tracking Efficiency for Indoor Light Energy Harvesting
Peng-Chang Huang, Tai-Haur Kuo
National Cheng Kung University, Taiwan

Abstract:
To harvest indoor light energy via photovoltaics (PVs), this paper proposes an adaptive-fractional-open-circuit-voltage (AFOCV) maximum power point tracking (MPPT) circuit to automatically adjust the FOCV fraction under different illuminances for amorphous PV modules. Designed in 0.5-μm CMOS process, the AFOCV circuit consumes an ultra-low average current of 100 pA. Over 100–1000 lux illuminance, the measured MPPT efficiency with AFOCV is >99.6%, which outperforms that of other state-of-the-art energy harvesting (EH) ICs with conventional FOCV methods.

Keywords: adaptive-fractional-open-circuit-voltage, AFOCV, energy harvesting, maximum power point tracking
Session 14: ADC Techniques

DATE/TIME: November 6, 2019 (Tuesday) / 1:40 PM – 3:20 PM
ROOM: 7404 & 7504
CHAIR: Qiang Li, University of Electronic Science and Technology of China
CO-CHAIR: Nan Sun, University of Texas at Austin

14 – 1 1:40 PM – 2:05 PM

A Single-Supply Buffer-Embedding SAR ADC with Skip-Reset Having Inherent Chopping Capability
Min-Jae Seo¹, Dong-Hwan Jin¹, Ye-Dam Kim¹, Jong-Pal Kim², Dong-Jin Chang¹, Won-Mook Lim¹, Jae-Hyun Chung¹, Chang-Un Park¹, Eun-Ji An¹, Seung-Tak Ryu¹
¹KAIST, Korea; ²Samsung Advanced Institute of Technology, Korea

Abstract:
This paper presents a power-efficient buffer-embedding successive approximation register (SAR) analog-to-digital converter (ADC) that utilizes a core power supply for the source-follower buffer having a rail-to-rail signal swing owing to the capacitive level shifting bias. In conjunction with 8x oversampling and the power-saving skip reset technique that has the inherent chopping capability, the prototype 180nm CMOS 12b ADC operating at 5.12 MS/s achieved 74.8 dB SNDR under a 1.5V supply voltage.

Keywords: low power, analog-to-digital converter (ADC), successive approximation register (SAR), loop-embedded input buffer, push-pull source follower

14 – 2 2:05 PM – 2:30 PM

A 68 dB SNDR Compiled Noise-Shaping SAR ADC with On-Chip CDAC Calibration
Harald Garvik², Carsten Wulff¹, Trond Ytterdal²
¹Nordic Semiconductor, Norway; ²Norwegian University of Science and Technology, Norway

Abstract:
This paper presents a noise-shaping SAR ADC with an on-chip, foreground capacitive DAC (CDAC) calibration system. At start-up, the ADC uses the LSBs in the CDAC to measure and digitize the errors of the MSBs. A synthesized digital module accumulates the noise-shaped measurements, computes calibration coefficients, and corrects ADC codes at run-time. The prototype is implemented in 28 nm FDSOI, and achieves 68.2 dB SNDR at 5 MHz bandwidth, while consuming 108.7 μW from a 0.8 V supply. The Walden FOM is 5.2 fJ/conv.-step. The layout of the ADC is compiled using an analog layout compiler.

Keywords: Noise-shaping, SAR, ADC, Noise-shaping SAR, CDAC calibration, analog layout synthesis

14 – 3 2:30 PM – 2:55 PM
A Digitally-Calibrated 70.98dB-SNDR 625kHz-Bandwidth Temperature-Tolerant 2nd-Order Noise-Shaping SAR ADC in 65nm CMOS
Jae Sik Yoon, Jiyoung Hong, Jintae Kim
Konkuk University, Korea

Abstract:
This paper presents a temperature-tolerant 2nd-order noise-shaping (NS) SAR ADC with a cascade of temperature-compensated dynamic amplifier and a ring amplifier to realize a low-power/low-noise feedback path gain. For a temperature-tolerant dynamic amplifier, we design the temperature-aware pulse generator using bandgap reference. A new mismatch calibration technique optimized for a noise-shaping SAR ADC is also presented. Fabricated in 65nm CMOS, the prototype ADC shows peak SNDR of 70.98dB with signal bandwidth of 625kHz. Over 70-degree of temperature range, it shows only 2dB SNDR drop, it achieves Walden FoM of FoMW=35.9f and Schreier FoM of FoMS=168dB, respectively.

Keywords: SAR ADC, Noise Shaping, Digital Calibration, Dynamic Amplifier

14 – 4 2:55 PM – 3:20 PM

8.6fJ/Step VCO-Based CT 2nd-Order ΔΣ ADC
Akshay Jayaraj1, Abhijit Das1, Srinivas Arcot2, Arindam Sanyal2
1Texas Instruments, United States; 2University at Buffalo, United States

Abstract:
A purely VCO-based continuous-time (CT), single loop second order delta sigma ADC is proposed in this work. Two ring oscillators are used as integrators to perform second-order quantization noise shaping. The proposed CT delta sigma ADC does not require additional circuit for excess loop delay compensation. A current reuse DAC architecture is proposed to simultaneously reduce ADC noise and power consumption. A 65nm prototype consumes 105uW from 1V supply at sampling frequency of 32.6MHz, and achieves a walden FoM of 8.6fJ/step over 2.3MHz bandwidth, which is the best among current CT delta sigma ADCs.

Keywords: voltage-controlled oscillator, analog-to-digital converter, delta-sigma, continuous-time ADC
A 110.3-Bits/Min 8-Ch SSVEP-Based Brain-Computer Interface SoC with 87.9% Accuracy
Wooseok Byun¹, Dokyun Kim³, Sung Yeon Kim³, Ji-Hoon Kim²
¹Chungnam National University, Korea; ²Ewha Womans University, Korea; ³Seoul National University of Science and Technology, Korea

Abstract:
This paper proposes 8-channel SSVEP-based visual target identification SoC to improve the ITR for low-cost wearable BCI device. The proposed target identification algorithm, CCA-CR based on canonical correlation analysis (CCA), includes algorithmic optimizations and candidate reduction (CR) method to reduce the signal processing load by at least 75% without degrading target identification accuracy and ITR. This paper also proposes matrix decomposition processor (MDP) that computes complex matrix arithmetic operations through systolic array based CCA-CR engines. Compared to the state-of-the-art CCA-based algorithm, the proposed SoC implemented in FPGA exhibits 63% better ITR with 33% reduction of recording time without accuracy degradation.

Keywords: brain-computer interface, system-on-chip, matrix decomposition, steady-state visual evoked potential, target identification

FPGA-Based Sparsity-Aware CNN Accelerator for Noise-Resilient Edge-Level Image Recognition
Seungsik Moon, Hyunhoon Lee, Younghoon Byun, Jongmin Park, Junseo Joe, Seokha Hwang, Sunggu Lee, Youngjoo Lee
Pohang University of Science and Technology, Korea

Abstract:
This paper presents a novel sparsity-aware CNN accelerator supporting the edge-level image recognition even for noisy images. In the proposed accelerator, we characterize the class of input noises by utilizing the FFT-based on-the-fly noise classifier. The proposed convolution engine then accesses the external memory to load the dedicated network that provides the accurate inference processing for the detected noise class. To save the energy consumed by the external DRAM accesses, in addition, we present the filter-level pruning algorithm with the memory-reduced indexing scheme, which can reduces the processing latency by utilizing the indexing method. To verify the effectiveness of the proposed methods, the proposed CNN
accelerator is implemented in the commercialized FPGA-based platform, achieving the processing rate of 57.6GOPS at the speed of 100MHz. Utilizing the dedicated network for each noise type, the prototype accelerator reduces the energy consumption by 62% compared to the conventional network with a similar recognition accuracy, which is suitable for the intelligent edge-level devices subjected to the various noises in practice.

Keywords: FPGA, CNN, Accelerator, Noise-resilient, Sparsity-aware

15 – 3 2:30 PM – 2:55 PM

Flexible Low Power CNN Accelerator for Edge Computing with Weight Tuning
Miaorong Wang, Anantha P. Chandrakasan
Massachusetts Institute of Technology, United States

Abstract:
This paper proposes a weight tuning algorithm to improve the energy efficiency of a NN accelerator by lowering the switching activity. A flexible CNN accelerator is co-designed with the algorithm and demonstrated with a feature extraction processor on an FPGA. The system is fully self-contained for small CNNs and speech keyword spotting is shown as an example. A fully integrated custom ASIC is also being fabricated for this system. Based on post P&R simulation of the ASIC, the weight tuning algorithm reduces the energy consumption of weight delivery and computation by 1.70x and 1.20x respectively with little loss in accuracy.

Keywords: Digital Accelerator, CNN, Deep Learning, Algorithm-and-Hardware Co-Design

15 – 4 2:55 PM – 3:20 PM

An Asynchronous Reconfigurable SNN Accelerator with Event-Driven Time Step Update
Jilin Zhang1, Hui Wu1, Jinsong Wei2, Shaojun Wei1, Hong Chen1
1Tsinghua University, China; 2University of Science and Technology of China, China

Abstract:
In this paper, we put forward an asynchronous spiking neural network (SNN) accelerator with 1024 neurons and 1 million synapses, which is reconfigurable in terms of network connection and neuron parameters. Bundled data asynchronous circuits are adopted to design the neuromorphic computation core and mesh network. Multicast communication is used to transmit packet among and within each core for less packet transmission and better energy efficiency. A novel time step update mechanism, which updates neurons in an event-driven manner without considering the chip-wide activity of other unrelated neurons, is proposed to improve the performance of speed. The SNN accelerator is verified by classifying MNIST handwritten digit with Xilinx VC707 FPGA. The results show that the accelerator achieves 98% accuracy with MINST database, and more than 1 GIPS/W energy efficiency which is 32 times better than previous work.

Keywords: SNN, asynchronous circuit, FPGA, neuromorphic computation
A 55nm 1-to-8 Bit Configurable 6T SRAM Based Computing-in-Memory Unit-Macro for CNN-Based AI Edge Processors
Zhixiao Zhang, Jia-Jing Chen, Xin Si, Yung-Ning Tu, Jian-Wei Su, Wei-Hsing Huang, Jing-Hong Wang, Wei-Chen Wei, Yen-Cheng Chiu, Je-Min Hong, Shyh-Shyuan Sheu, Sih-Han Li, Ren-Shuo Liu, Chih-Cheng Hsieh, Kea-Tiong Tang, Meng-Fan Chang
1Industrial Technology Research Institute, Taiwan; 2National Tsing Hua University / Industrial Technology Research Institute, China; 3National Tsing Hua University, Taiwan

Abstract:
A 4Kb configurable 6T-SRAM CIM unit-macro was fabricated using a 55nm CMOS process and foundry 6T cells. The resulting macro achieved 3.5ns access time with 3b PS outputs and gained a 3.91-50x improvement in figure-of-merit, compared to previous SRAM-CIMs.

Keywords: CIM, SRAM, CNN, AI edge processor
Configurable BCAM/TCAM Based on 6T SRAM Bit Cell and Enhanced Match Line Clamping
Jongeun Koo, Eunhwan Kim, Seunghyun Yoo, Taesu Kim, Sungju Ryu, Jae-Joon Kim
Pohang University of Science and Technology, Korea

Abstract:
We present a configurable 6T binary content-addressable memory (BCAM) and 12T ternary CAM (TCAM) which is based on conventional 6T SRAM bit cell. We also propose a match line (ML) voltage/current clamping scheme to reduce ML discharge delay considerably while preventing data corruption during CAM search operation compared to the previous configurable BCAM/TCAM using 6T SRAM bit cell. Experimental data from 4Kb (64x64b) CAM testchips in a 28nm CMOS technology shows that the proposed ML clamping scheme achieves 53.7% reduction in ML discharge delay compared to the previous word line underdrive scheme.

Keywords: Memory, SRAM, CAM

Sub-ns Access Sub-mW/GHz 32 Kb SRAM with 0.45 V Cross-Point-5T Cell and Built-in Y_line
Chen-Yu He², Kuei-Hua Tang², Tsung-Shen Chen¹, Kang-Yu Chang², Chien-Hung Lin², Katsuyuki Sato², Shyh-Jye Jou², Po-Hung Chen², Hung-Ming Chen², Bor-Doou Rong¹, Kiyoo Itoh²
¹Etron Technology Inc., Taiwan; ²National Chiao Tung University, Taiwan

Abstract:
A 0.45 V 28-nm 32-Kb SRAM with multi-power-supply low-power circuits, such as a cross-point 5T with built-in Y_line, gate-boosted drivers and adaptive tracking circuits, demonstrates a sub-ns access time and sub mW/GHz power dissipation. The 5T circuits are feasible to reduce the power of a 6T 32-Kb core to about 30% with quite the same sub-ns access time. The performance evaluation also indicates the new bit cell and array architecture open the door to the sub-ns access time and sub mW/GHz in sub-0.5 V multi-Mb era.

Keywords: Sub-0.5 V SRAM, 5T bit (memory) cell, gate-boosting driver, low-power array
Privacy-Aware Data-Lifetime Control NAND Flash System for Right to be Forgotten with In-3D Vertical Cell Processing
Shun Suzuki, Kyoji Mizoguchi, Hikaru Watanabe, Toshiki Nakamura, Yoshiaki Deguchi, Keita Mizushina, Ken Takeuchi
Chuo University, Japan

Abstract:
This paper proposes Privacy-aware Data-Lifetime Control NAND Flash System (PDLCS), which changes the data-lifetime flexibly for the right to be forgotten. This system realizes both short and long term data-lifetime by In-3D Vertical Cell Processing. Furthermore, data-lifetime can be extended or shortened at any time. This system secures privacy data and thus is a universal solution for future secure storage, which is not resolved by software techniques.

Keywords: 3D NAND flash memories, Security, Privacy data, Lifetime control, Vertical charge de-trap, Lateral charge migration
**Session 17: High-Speed Wireline Receiver**

**DATE/TIME:** November 6, 2019 (Tuesday) / 1:40 PM – 3:20 PM  
**ROOM:** 7405 & 7505  
**CHAIR:** Nan Qi, Institute of Semiconductors, Chinese Academy of Sciences  
**CO-CHAIR:** Peng Liu, Zhejiang University

**17 – 1  1:40 PM – 2:05 PM**

**A 1.64mW Differential Super Source-Follower Buffer with 9.7GHz BW and 43dB PSRR for Time-Interleaved ADC Applications in 10nm**

Yizhak Shifman, Yoel Krupnik, Udi Virobnik, Ahmad Khairi, Yosi Sanhedrai, Ariel Cohen  
*Intel Corporation, Israel*

**Abstract:**  
A differential buffer for high bandwidth (BW), Time-Interleaved Analog to Digital Converters (TI ADCs) is described. The buffer, nested between Track and Hold (TH) circuits, drives the ADC input signal to the individual sub ADCs. A differential, super source-follower based architecture is utilized in the buffer. This architecture features high power supply rejection ratio (PSRR) together with high BW, low power consumption and low Inter-Symbol Interference (ISI). The buffer was fabricated in 10nm Intel process as a part of a 112Gbps SerDes receiver. A unique method was developed to accurately measure the buffer’s output waveform. Measurements show a BW of 9.7GHz, PSRR of 43dB and power consumption of 1.64mW, which is a 68% power reduction compared to the prior art.

**Keywords:** Buffer, Source Follower, Time Interleaved ADC

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**17 – 2  2:05 PM – 2:30 PM**

**A 4.8pJ/B 56Gb/s ADC-Based PAM-4 Wireline Receiver Data-Path with Cyclic Prefix in 14nm FinFET**

Gain Kim⁵, Lukas Kull¹, Danny Luu¹, Matthias Braendli³, Christian Menolfi¹, Pier-Andrea Francese³, Hazar Yueksel⁰, Cosimo Aprile², Thomas Morf², Marcel Kossel³, Alessandro Cevrero³, Ilter Ozkaya², Hyeon-Min Bae³, Andreas Burg², Thomas Toifl¹, Yusuf Leblebici²  
¹Cisco Systems (Switzerland) GmbH, Switzerland; ²École Polytechnique Fédérale de Lausanne, Switzerland; ³IBM Research Zurich Laboratory, Switzerland; ⁴IBM T. J. Watson Research Center, United States; ⁵KAIST, Korea

**Abstract:**  
This work presents an ADC-based receiver (RX) data-path for frame-based PAM-4 modulation with a cyclic prefix (CP). Similar to discrete multi-tone (DMT) modulation, a frame of PAM-4 symbols are protected from the channel delay spread by the CP taps. A PAM-4 frame window including CP taps is viewed as a DMT symbol and is equalized similarly to a DMT signal equalization, based on a discrete-time Fourier transform (DFT) and frequency-domain equalizer (FDE). The RX prototype implemented in 14nm FinFET achieves 56Gb/s data-rate at less than 3e-5 pre-FEC BER over a 19dB loss channel at 14GHz dissipating 270mW including the ADC and the DSP data-path excluding the inverse DFT and the BER checker.
Keywords: Wireline, receiver, serial-data transceiver, PAM-4, discrete multi-tone, DMT, SerDes

17 – 3  2:30 PM – 2:55 PM
A 32-Gb/s 0.46-pJ/bit PAM4 CDR Using a Quarter-Rate Linear Phase Detector and a Low-Power Multiphase Clock Generator
Zhao Zhang, Guang Zhu, Can Wang, Li Wang, C. Patrick Yue
Hong Kong University of Science and Technology, China

Abstract:
This paper presents a low-power low-jitter PAM4 clock and data recovery circuit. A novel quarter-rate linear phase detector (QLPD) is proposed to lower the recovered clock jitter. A self-biased PLL based multiphase clock generator (MCG) is proposed to reduce power consumption. Fabricated in 40-nm CMOS process, the prototype achieves error-free operation at 32-Gb/s input data rate with 0.46-pJ/bit bit efficiency and 352.6- fs integrated jitter of the 4-GHz recovered clock. The measured jitter tolerance at BER of <10-12 is higher than 0.35 UIPP with the corner frequency at about 10 MHz.

Keywords: PAM CDR, quarter-rate linear phase detector, multiphase clock generator, low-power, self-biased PLL

17 – 4  2:55 PM – 3:20 PM
A Maximum-Eye-Tracking CDR with Biased Data-Level and Eye Slope Detector for Optimal Timing Adaptation
Hye-Yoon Joo1, Deog-Kyoon Jeong2
1Seoul National University, Korea; 2Seoul National University / Samsung Electronics, Korea

Abstract:
In this paper, a maximum-eye-tracking CDR (MET-CDR) for minimum bit error rate (BER) is presented. The proposed CDR does not require a BER counter or eye-opening monitor to find the optimal sampling phase. The biased data-level obtained from the weighted sum of UP and DN is proposed to extract the actual eye height information considering the pre-cursor ISI. Two error samples with small time spacing detect the current eye height and the slope of the eye height so that the CDR tracks the maximum eye height where the slope becomes zero. Measured results prove that the maximum eye height phase and the minimum BER phase matches well. A prototype receiver fabricated in 28-nm CMOS process operates at 26Gb/s with an eye-opening of 25% UI and consumes 87mW while equalizing 21dB of loss at 13GHz.

Keywords: clock and data recovery (CDR), pre-cursor intersymbol interference (ISI), sampling point control, timing adaptation
A 200-MHz Wide Input Range CMOS Passive Rectifier with Active Bias Tuning
Xiaofei Li¹, Fangyu Mao², Pyungwoo Yeon¹, Yan Lu², Maysam Ghovanloo¹, Rui P. Martins³
¹Georgia Institute of Technology, United States; ²University of Macau, Macau; ³University of Macau / Universidade de Lisboa, Macau

Abstract:
A high efficiency wireless power transfer system that operates in the very high frequency (VHF) band is desirable for miniaturized implantable medical devices, but also challenging. This work presents an integrated VHF passive rectifier with closed-loop active bias tuning (ABT). Power PMOS and NMOS transistors are separately cross-connected, such that the DC bias voltages of the NMOS gates can be dynamically adjusted. A searching scheme for VOUT-peak is employed to obtain the optimum bias voltage over a wide input range. A prototype is fabricated in 65nm standard CMOS process with a measured power convention efficiency of 64% at 200MHz with 3kΩ loading.

Keywords: Active bias tuning, wireless power transfer, rectifier, implantable medical devices, VHF

A 7.5 - 42V Input High-VCR Monolithic DC-DC Converter Using Stacked Isolated SC Cores
Elly De Pelecijn, Michiel Steyaert
Katholieke Universiteit Leuven, Belgium

Abstract:
A fully integrated switched-capacitor DC-DC power converter that converts input voltages up to 42 V into 3 V is presented. The converter achieves a wide input operating range with multiple VCRs based on stacking of several isolated switched-capacitor converters. Stacking simplifies the design to a low voltage unit converter with only a few VCRs, while the wide input range high voltage converter achieves the high efficiency of the unit converter. The DC-DC converter is designed in a 0.35 um CMOS technology and achieves an output power of 2.1 mW.

Keywords: Stacking, DC-DC converter, Switched-Capacitor, Wide input range, High VCR, Isolated converter, Monolithic
18 – 3 (Short Paper)  4:40 PM – 4:52 PM

A 918MHz Wide-Range CMOS Rectifier with Diode-Feeding and Switch-Capacitor-Based Load Modulation Technique
Chen-Yi Kuo, Chun-An Lu, Yu-Te Liao
National Chiao Tung University, Taiwan

Abstract:
This paper presents a wide-input-range rectifier design with a diode-feeding (DF) architecture and load modulation. Dynamically-biased diodes are connected to the gates of the rectifying transistors to create bias voltage differences for PMOS and NMOS devices and the isolation of the reverse currents at different input power levels. Also, the switch-capacitor-based load modulation scheme is proposed to achieve optimal efficiency over wide-range load current deviations automatically. The proposed four-stage rectifier design was fabricated using 65nm CMOS technology and occupies a silicon area of 0.92 x 0.27mm². The measured sensitivity of the rectifier is −15dBm at 1MΩ load, and the peak power conversion efficiency is 28% at a load of 22kΩ. With the load modulation scheme, the conversion efficiency is enhanced by >10% in a load current from 7μA to 35μA, when compared to a design without the load modulation scheme.

Keywords: Rectifier, RF energy harvesting, wireless powering

18 – 4 (Short Paper)  4:52 PM – 5:05 PM

A CMOS Switched-Capacitor Boost Mode Envelope Tracking Regulator with 4% Efficiency Improvement at 7.7dB PAPR for 20MHz LTE Envelope Tracking RF Power Amplifiers
Neha Kumari¹, Shang-Hsien Yang¹, Ke-Horng Chen¹, Ying-Hsi Lin², Shian-Ru Lin², Tsung-Yen Tsai²
¹National Chiao Tung University, Taiwan; ²Realtek Semiconductor Corp, Taiwan

Abstract:
In this paper, the switched-capacitor boost (SCB) mode envelope tracking (ET) technique with a switched-capacitor circuit and a low dropout (LDO) regulator are used to replace conventional envelope tracking regulators. At a Peak-to-Average Power Ratio (PAPR) of 7.7dB common for LTE communication, the efficiency is 72%, which is 4% higher than the theoretical limit of conventional ET techniques. When PAPR increases from 6.1dB to 7.3dB, the conventional ET efficiency decreases from 82% to 69% whereas the SCB mode increases by 2%.

Keywords: envelope tracking (ET), Peak-to-Average Power Ratio (PAPR), switched-capacitor boost (SCB)

18 – 5  5:05 PM – 5:30 PM

A Conversion-Ratio-Insensitive High Efficiency Soft-Charging-Based SC DC-DC Boost Converter for Energy Harvesting in Miniature Sensor Systems
Junyoung Park², Hyungmin Gi², Seungchul Jung¹, Sang Joon Kim¹, Yoonmyung Lee²
¹Samsung Advanced Institute of Technology, Korea; ²Sungkyunkwan University, Korea
Abstract:
A switched-capacitor (SC) DC-DC boost converter suitable for energy harvesting in IoT sensor systems with varying harvesting source and battery voltages is presented in this paper. Unlike the conventional multi-staged SC DC-DC converters, where efficiency is optimized only for a few topology-dependent conversion ratios, soft-charging-based SC conversion is adopted to achieve conversion-ratio-insensitive high efficiency. With soft-charging flying capacitors with small voltage steps, charge re-distribution loss is minimized and evenly high conversion efficiency can be achieved for a wide range of input and output voltages. The proposed converter exhibited evenly high efficiency by achieving a peak efficiency of 85.3% and an average efficiency of 83.6% for generating regulated 1.8V output from a wide range of input voltages (0.9–1.8V). It also achieved a peak efficiency of 88.9% and an average efficiency of 87.6% for harvesting energy from a 1.2V source with a wide battery voltage range (3.0–4.2V).

Keywords: soft-charging, switched capacitor, boost converter, DC-DC converter, charge redistribution
Session 19: Low Power SoC for IoT
DATE/TIME: November 6, 2019 (Wednesday) / 3:50 PM – 5:30 PM
ROOM: 7404 & 7504
CHAIR: Daisuke Mizoguchi, Renesas
CO-CHAIR: Yun Chen, Fudan University

19 – 1  3:50 PM – 4:15 PM

33us, 94uJ Optimal Ate Pairing Engine on BN Curve Over 254b Prime Field in 65nm CMOS FDSOI
Makoto Ikeda, Tadayuki Ichihashi, Hiromitsu Awano
University of Tokyo, Japan

Abstract:
We have designed optimal ate paring engine on BN curve over 254bit prime field in 65nm CMOS FDSOI process. Algorithm is broken down into 2nd extension of the prime field (Fp2) and optimized for pipelined multiplier of Fp2, results in global optimum design. Measurement results demonstrate world fastest implementation of 33us paring time with as low as 94uJ per paring. Energy consumption can be minimized down to 13.7uJ per pairing for 490mV operation. The design consists of 2.8MG and 85% of functional units are active throughout the paring operation. The demonstrated results are promising to realize functional encryptions such like ID based encryption, attribute-based encryption and searchable encryption.

Keywords: Optimal ate paring, BN curve, 254bit prime field, 65nm CMOS, crypto engine design, and functional encryption

19 – 2  4:15 PM – 4:40 PM

An IoT Sensor Node SoC with Dynamic Power Scheduling for Sustainable Operation in Energy Harvesting Environment
Yuji Yano³, Seiya Yoshida³, Shintaro Izumi³, Hiroshi Kawaguchi³, Tetsuya Hirose⁴, Masaya Miyahara², Teruki Someya⁵, Kenichi Okada⁵, Ippei Akita¹, Yoshihiko Kurui⁶, Hideyuki Tomizawa⁶, Masahiko Yoshimoto³
¹Advanced Industrial Science and Technology, Japan; ²High Energy Accelerator Research Organization, Japan; ³Kobe University, Japan; ⁴Osaka University, Japan; ⁵Tokyo Institute of Technology, Japan; ⁶Toshiba Corporation, Japan

Abstract:
This paper describes a low-power IoT sensor node SoC that can be used for factory automation and wearable healthcare applications. It features dynamic power scheduling method suitable for the environment that works with an energy harvester. A mixed-signal SoC has been fabricated using the TSMC 65 nm LP process. The prototype SoC equipped with dynamic power scheduling consumes about 3.4 μW when the activity ratio is 0.1%. Evaluation results show that the proposed method can reduce about 51% of the power consumption of sensor node SoC.
A 3.01 mm² 65.38Gb/s Stochastic LDPC Decoder for IEEE 802.3an in 65 nm
Qichen Zhang¹, Yun Chen¹, Xiaoyang Zeng¹, Keshab K. Parhi³, Borivoje Nikolic²
¹Fudan University, China; ²University of California, Berkeley, United States; ³University of Minnesota, United States

Abstract:
A fully-parallel high-throughput LDPC decoder architecture leads to high power consumption and large area. Using stochastic logic, this paper proposes three novel strategies to improve throughput and reduce power consumption; these include: variable node initialization, bit-flipping post-processing and posterior-information-based hard decision. Moreover, a random number based probability stochastic sequences generator is proposed to reduce hardware resources. Chip test results from an LDPC decoder for the 10GBASE-T standard (2048, 1723) code using 65 nm CMOS process demonstrate a 74.3% reduction in average decoding cycles at 4.4 dB with satisfactory decoding performance. The decoder supports 65.38 Gb/s throughput at 420 MHz and requires 1.1W power consumption. Compared with other works, the proposed decoder can achieve lower power and average decoding cycles with similar error performance.

Keywords: Stochastic computation, High throughput decoder, Bit-Flipping algorithm

A Millimeter Wave Digital CMOS Baseband Transceiver for Wireless LAN Applications
Kang-Lun Chiu³, Hsun-Wei Chan³, Wei-Che Lee³, Chang-Ting Wu³, Henry Lopez³, Hung-Chih Liu³, Meng-Yuan Huang², Chun-Yi Liu³, Tsai-Hua Lee³, Hsin-Ting Chang³, Chih-Wei Jen³, Nien-Hsiang Chang¹, Pei-Yun Tsai², Yen-Cheng Kuan³, Shyh-Jye Jou³
¹National Applied Research Laboratories, Taiwan; ²National Central University, Taiwan; ³National Chiao Tung University, Taiwan

Abstract:
We introduce a 10 Gbps digital baseband transceiver with 16-QAM, 3/4 code rate single carrier mode under 28 nm CMOS process implementation. In millimeter wave communications, IEEE 802.11ad standard is referenced for our design. We target at 2.5 GHz chip rate with 4 times parallelism hardware at clock rate 625 MHz. We achieve the required bit error rate 3e-7 before SNR 18.5 dB. We implement the hardware with the core area 2.92 mm² with measured power 1.8 Watt for baseband transceiver chip. The performance of energy per bit is 0.023 nJ and 0.211 nJ per bit for Tx and Rx, including ADC/DAC.

Keywords: mmWave, Single Carrier (SC), Digital Baseband, IEEE 802.11ad/ay
A 23-mW 60-GHz Differential Sub-Sampling PLL with an NMOS-Only Differential-Inductively-Tuned VCO
Bingwei Jiang, Howard Luong
_Hong Kong University of Science and Technology, Hong Kong_

Abstract:
A 60-GHz sub-sampling PLL (SSPLL) employs a differential tuning loop to suppress the reference spur. The VCO frequency is differentially tuned only by NMOS transistors. An injection-locked frequency divider (ILFD) with a 4th-order resonant tank is employed between the VCO and the phase detector (PD) to further minimize the spur even without an isolation buffer. Fabricated in 65nm CMOS, the prototyped differential SSPLL measures RMS jitter of 236 fs and reference spur from -43 to -52-dBc over a frequency tuning range from 55.5 to 60 GHz while consuming 23mW from xx-V supply corresponding to FOM of -238.9dB.

Keywords: Sub-sampling PLL, phase noise, differential tuned VCO, injection-locked divider

A 0.003-mm² 440fsRMS-Jitter and -64dBc-Reference-Spur Ring-VCO-Based Type-I PLL Using a Current-Reuse Sampling Phase Detector in 28-nm CMOS
Zunsong Yang¹, Yong Chen¹, Pui-In Mak¹, Rui P. Martins²
¹_University of Macau, China_; ²_University of Macau / Universidade de Lisboa, China_

Abstract:
This paper reports a current-reuse sampling phase detector for a type-I phase-locked loop (PLL) to simultaneously achieve both wide loop bandwidth and low control voltage ripple, resulting in low RMS jitter and reference spur, while minimizing the chip area by avoiding an explicit loop filter. Fabricated in 28-nm CMOS, the PLL prototype measures a jitter of 440 fsRMS, and a spur level of -64 dBc at 3.296 GHz. The die area is 0.003 mm².

Keywords: Ring voltage-controlled oscillator (VCO), phase locked loop (PLL), reference spur, RMS jitter, phase detector.
A 360-456 MHz PLL Frequency Synthesizer with Digitally Controlled Charge Pump Leakage Calibration
Peilin Yang, Yanshu Guo, Hanjun Jiang, Zhihua Wang
Tsinghua University, China

Abstract:
This paper presents a 435MHz fractional-N mode frequency synthesizer in 65nm technology utilizing a hybrid compensation method against incorporated differential charge pump and loop filter leakages. This hybrid method takes advantages from its digital part realizing an accurate and flexible feedback compensation. Two-stages ring oscillator and multiphase divider are adopted to achieve smaller area and lower fractional division noise. Reference spur is reduced to -59.53dBc by 20dB. The phase noise is -92.99dBc/Hz at 1MHz offset. The power consumption is 1.153mW under 1V supply and the circuit area is 0.064mm^2.

Keywords: Frequency synthesizer, Fractional-N, Hybrid path, Leakage compensation, Negative resistance

A 12-GHz All-Digital Calibration-Free FMCW Signal Generator Based on a Retiming Fractional Frequency Divider
Zhengkun Shen, Heyi Li, Haoyun Jiang, Zherui Zhang, Junhua Liu, Huailin Liao
Peking University, China

Abstract:
A 12-GHz all-digital calibration-free frequencymodulated continuous-wave (FMCW) signal generator is presented in this paper based on a retiming fractional frequency divider (FFD). Instead of modulating a multi-modulus divider (MMD) by a ΔΣ modulator, a fractional divider is utilized to release the narrow loop bandwidth limitation and achieve better phase noise performance without active noise cancellation techniques. Thus, the FMCW signal generator can achieve low root-mean-square (RMS) frequency error under a fast chirp slop. A calibration-free retiming FFD architecture which is not sensitive to process, voltage and temperature (PVT) variations is proposed to avoid complex and slow calibration process. Implemented in 40 nm CMOS, the generator consumes 33.8 mW power and 0.32 mm2 chip area. Measurement results show that the generator achieves 78 MHz/μs maximum chirp slope and 6.0 kHz RMS frequency error when 300 MHz frequency is swept in 2 ms. The phase noise from 12 GHz carrier is -113.6 dBC/Hz at 1 MHz offset.

Keywords: All-digital PLL, Calibration-free, Frequencymodulated continuous-wave (FMCW), Radar, Fractional frequency divider
A 100Mb/s 3.5GHz Fully-Balanced BFOOK Modulator Based on Integer-N Hybird PLL
Cong Ding, Haixin Song, Woogeun Rhee, Zhihua Wang
Tsinghua University, China

Abstract:
This paper presents an energy-efficient high data rate constant-envelope modulator by employing a binary frequency-domain on-off keying (BFOOK) method. Thanks to the fully-balanced FSK feature, high data rate BFOOK modulation is performed based on an integer-N hybrid PLL with VCO modulation only. A carrier spreading technique based on low-frequency wideband triangular modulation can also be added as an optional fractional-N mode in case carrier power suppression is needed to have better spectrum compliance. A prototype 3.5GHz modulator is implemented in 65nm CMOS. The BFOOK modulator achieves the maximum data rate of 100Mb/s, maintaining averaged center frequency regardless of the data pattern. The modulator consumes 9.6mW from a 1V supply, achieving the energy efficiency of 96pJ/b.

Keywords: PLL, FSK, FOOK, energy efficiency.

Session 21: Biomedical Sensor Interfaces
DATE/TIME: November 6, 2019 (Wednesday) / 3:50 PM – 5:30 PM
ROOM: 7501 AB
CHAIR: Pui-In Mak, University of Macau
CO-CHAIR: Masaki Sakakibara, Sony Semiconductor Solutions Corporation

A 15-Ch. 0.019 mm²/Ch. 0.43% Gain Mismatch Orthogonal Code Chopping Instrumentation Amplifier SoC for Bio-Signal Acquisition
Jeong Hoan Park¹, Tao Tang², Lian Zhang², Kian Ann Ng¹, Jerald Yoo³
¹N.1 Institute for Health, Singapore; ²National University of Singapore, Singapore; ³National University of Singapore / N.1 Institute for Health, Singapore

Abstract:
This paper proposes a 15-Ch. low power, small area, Orthogonal Code Chopping Instrumentation Amplifier (OCCIA). Orthogonal codes directly modulate each channel and merge into a single IA while performing dynamic offset compensation. Digitization-Before-Demodulation (DBD) transmits the combined data directly, which alleviates ripple noise, and completely removes the demodulation and TX encoding overhead from the SoC. The proposed OCCIA SoC in 0.18μm 1P6M CMOS achieves the lowest gain mismatch (0.43%) among recent multi-channel IAs with one of the smallest areas (0.019mm2/ch.) while consuming 1.97μW/ch. and low crosstalk (<-53.5dB) at 490Hz bandwidth.

Keywords: Bio-signal acquisition, demodulation-before-digitization, instrumentation amplifier, orthogonal code chopping
A 10 µW, −74.6 dB THD Arterial Pulse Waveform Sensing System with Automatic Bridge-Offset Calibration and Super Class-AB Output Stage
Yu-Pin Hsu, Zemin Liu, Mona Hella
Rensselaer Polytechnic Institute, United States

Abstract:
This paper presents a power-efficient, highly-linear sensing system for arterial pulse waveform (APW) acquisition. The system consists of a front-end circuit connected to a packaged silicone-coated resistive-bridge pressure sensor for detecting APW through direct skin contact in a non-invasive manner. Compared to other pulse sensing approaches, the proposed front-end only requires an instrumentation amplifier (IA) and a LPF-ADC, and consumes a total power of 10 µW. An automatic calibration circuit is proposed to compensate for the resistive-bridge offset and can reduce such offset down to 1 mV. High linearity in the IA is provided through the use of a super class-AB output stage. A LPF-ADC architecture is employed to extract and digitize the APW in a 100 Hz bandwidth, saving 90% of the passives area. The front-end provides a measured input-referred noise of 7.2 µVrms with a gain of 32–40 dB, and a THD of −74.6 dB. Together with an on-chip low dropout regulator (LDO) and a buffer stage, the prototype fabricated in 0.18 µm CMOS technology has an active area of 0.52 mm*mm.

Keywords: Blood Pressure, Sensor Interface, IA, DDA, Calibration, Pressure Sensor

A 0.012 mm², 1.5 GΩ ZIN Intrinsic Feedback Capacitor Instrumentation Amplifier for Bio-Potential Recording and Respiratory Monitoring
Lian Zhang¹, Tao Tang¹, Jeong Hoan Park¹, Jerald Yoo²
¹National University of Singapore, Singapore; ²National University of Singapore / N.1 Institute for Health, Singapore

Abstract:
An Intrinsic Feedback Capacitor Instrumentation Amplifier (IFCIA) is presented for bio-potential recording and respiratory monitoring. Exploiting the intrinsic gate-to-drain capacitor to scale down input capacitor, combined with interdigitated MOM capacitors, the inverter-based instrumentation amplifier (IA) occupies smallest active area of 0.012 mm² with 1.5 GΩ input impedance (> 1 GΩ up to 100 Hz) and 0.65 µA current consumption, while maintaining die-to-die gain mismatch of 0.41%.

Keywords: Analog front-end, bio-potential recording, impedance boosting, intrinsic feedback capacitor instrumentation amplifier, respiratory monitoring
T/R-Switch Composed of 3 High-Voltage MOSFETs with 12.1 μW Consumption That Can Perform Per-Channel TX to RX Self-Loopback AC Tests for 3D Ultrasound Imaging with 3072-Channel Transceiver
Shinya Kajiyama, Yutaka Igarashi, Toru Yazaki, Yusaku Katsube, Takuma Nishimoto, Tatsuo Nakagawa, Yohei Nakamura, Yoshihiro Hayashi, Taizo Yamawaki
Hitachi, Ltd., Japan

Abstract:
This paper presents an area- and power-efficient TX/RX-isolation switch implemented in a 3072-ch ultrasound transceiver IC. The proposed dynamic gate-source shunt topology, which utilizes a negative-HV-transmit-driven shunt switch, eliminates area- and power-hungry HV level shifters and ensures OFF during TX periods. In addition, source-driven HV-PMOS for ON/OFF control enables both gate charging and discharging using single HV-PMOS, thus contributing to area reduction. Moreover, by preparing an attenuation mode, a per-channel TX to RX self-loopback test can be performed. This function provides an on-wafer AC test without probing 3072 electrodes and can be applied to field diagnosis of assembled ultrasound probes.

Keywords: ultrasound, 3D imaging, 2D-array, matrix transducer, beamformer, T/R-switch, HV-switch, loopback test

A High DR High-Input-Impedance Programmable-Gain ECG Acquisition Interface with Non-Inverting Continuous Time Sigma-Delta Modulator
Junhao Liang2, Sai-Weng Sin2, Seng-Pan U2, Franco Maloberti4, Rui P. Martins3, Hanjun Jiang1
1Tsinghua University, China; 2University of Macau, Macau; 3University of Macau / Universidade de Lisboa, Macau; 4University of Pavia, Italy

Abstract:
This paper presents a power-efficient, high dynamic range, high input impedance data acquisition circuit for an implantable electrocardiogram (ECG) detector in 65 nm CMOS, occupying an active area of 0.225 mm2. To enhance the dynamic range, we utilize a 3rd-order continuous-time sigma-delta modulator with a programmable input gain coefficient and an embedded antialiasing filter. The implementation of the non-inverting integrator allows a high input impedance for the ECG application.

Keywords: Programmable gain amplifier, high input impedance, non-inverting integrator, ECG